[FIG. 1]

Structure of a conventional parallel processor

FIG.1 PRIOR ART

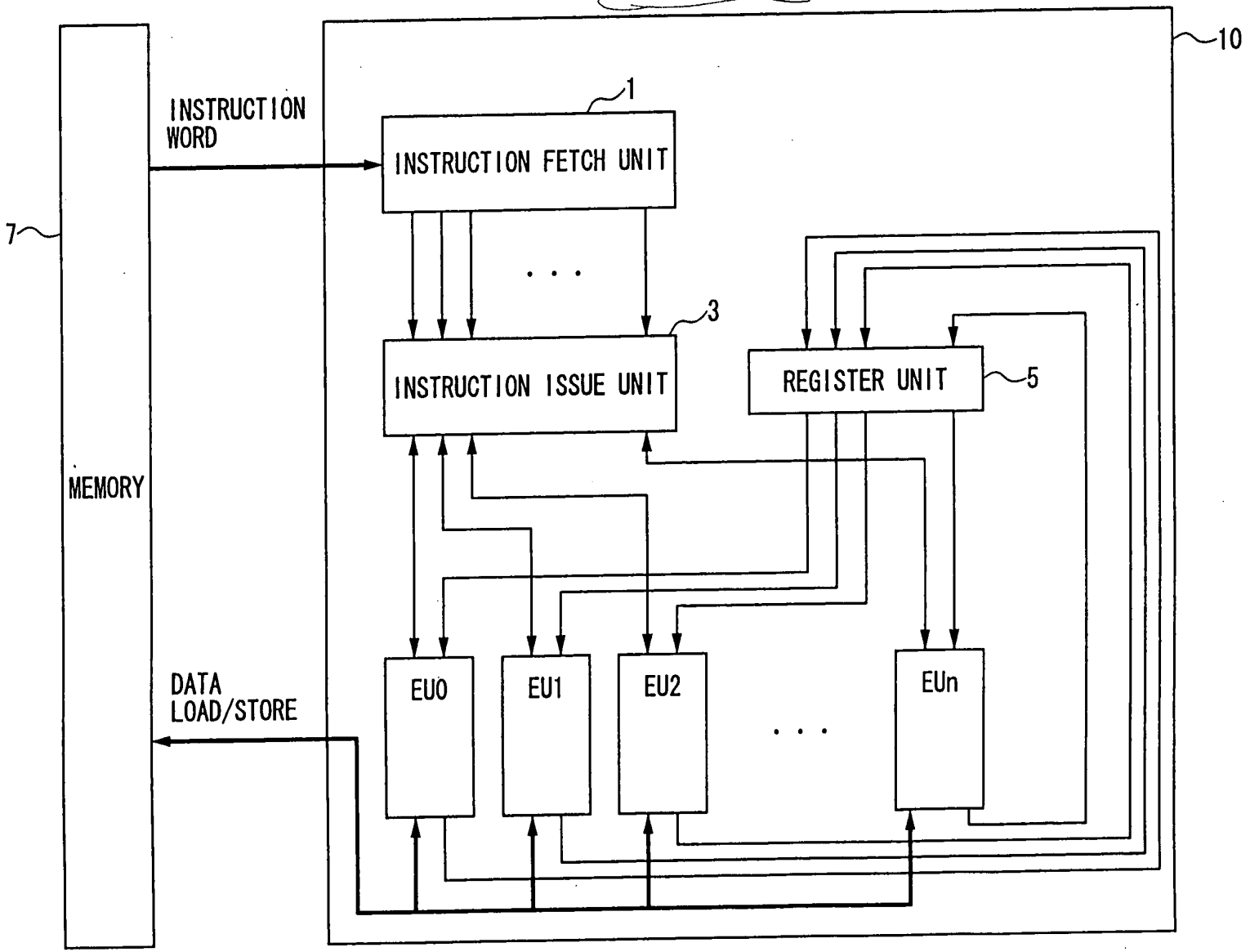


FIG.2

NOP	NOP	NOP	NOP
E1	NOP	NOP	NOP
NOP	E1	NOP	NOP
NOP	NOP	E1	NOP
NOP	NOP	NOP	E1
E1	E1	NOP	NOP
E1	NOP	E1	NOP
E1	NOP	NOP	E1
NOP	E1	E1	NOP
NOP	E1	NOP	E1
NOP	NOP	E1	E1
E1	E1	E1	NOP
E1	E1	NOP	E1
E1	NOP	E1	E1
NOP	E1	E1	E1
E1	E1	E1	E1

[FIG. 2]

Formats of instruction words to be supplied to a conventional parallel processor having four instruction execution units

[~~FIG. 3~~]

Structure of a first example of a parallel processor in accordance with a first embodiment of the present invention

FIG.3

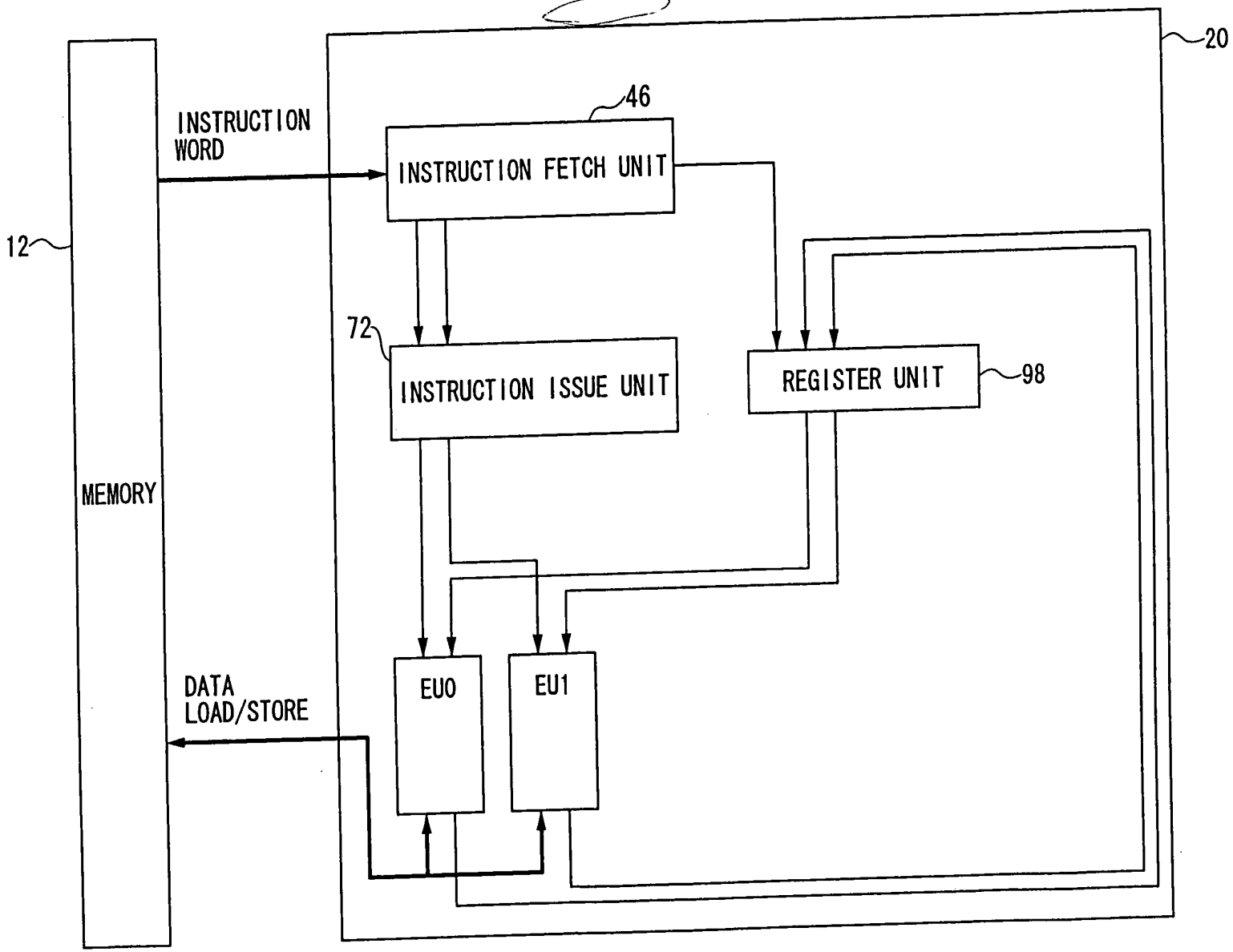
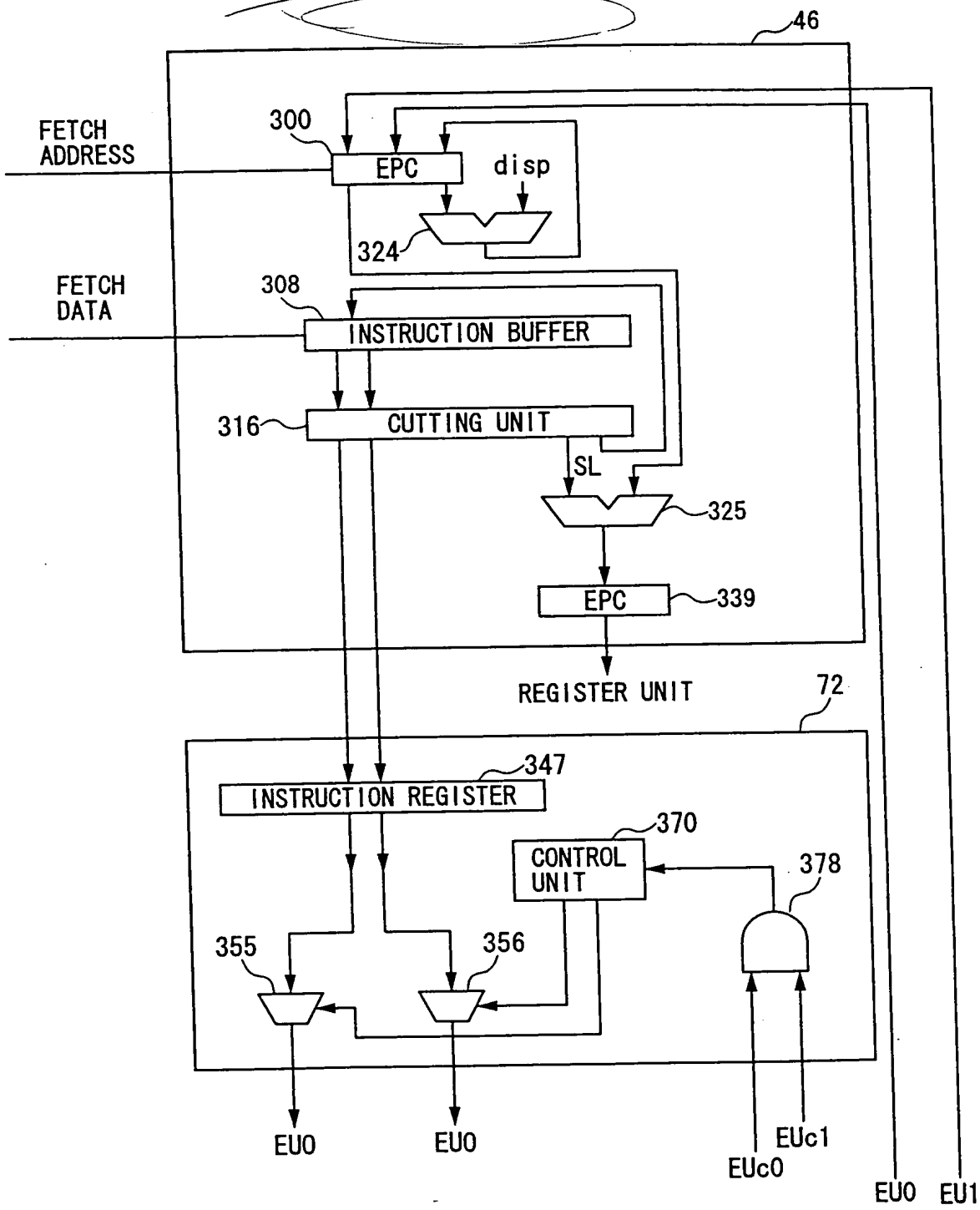


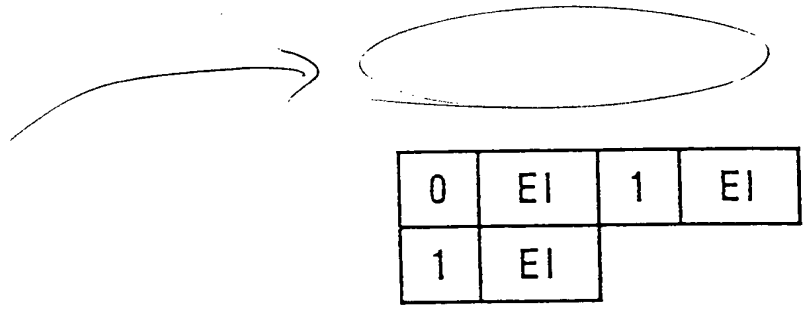
FIG.4



[~~FIG. 4~~]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 3

FIG. 5



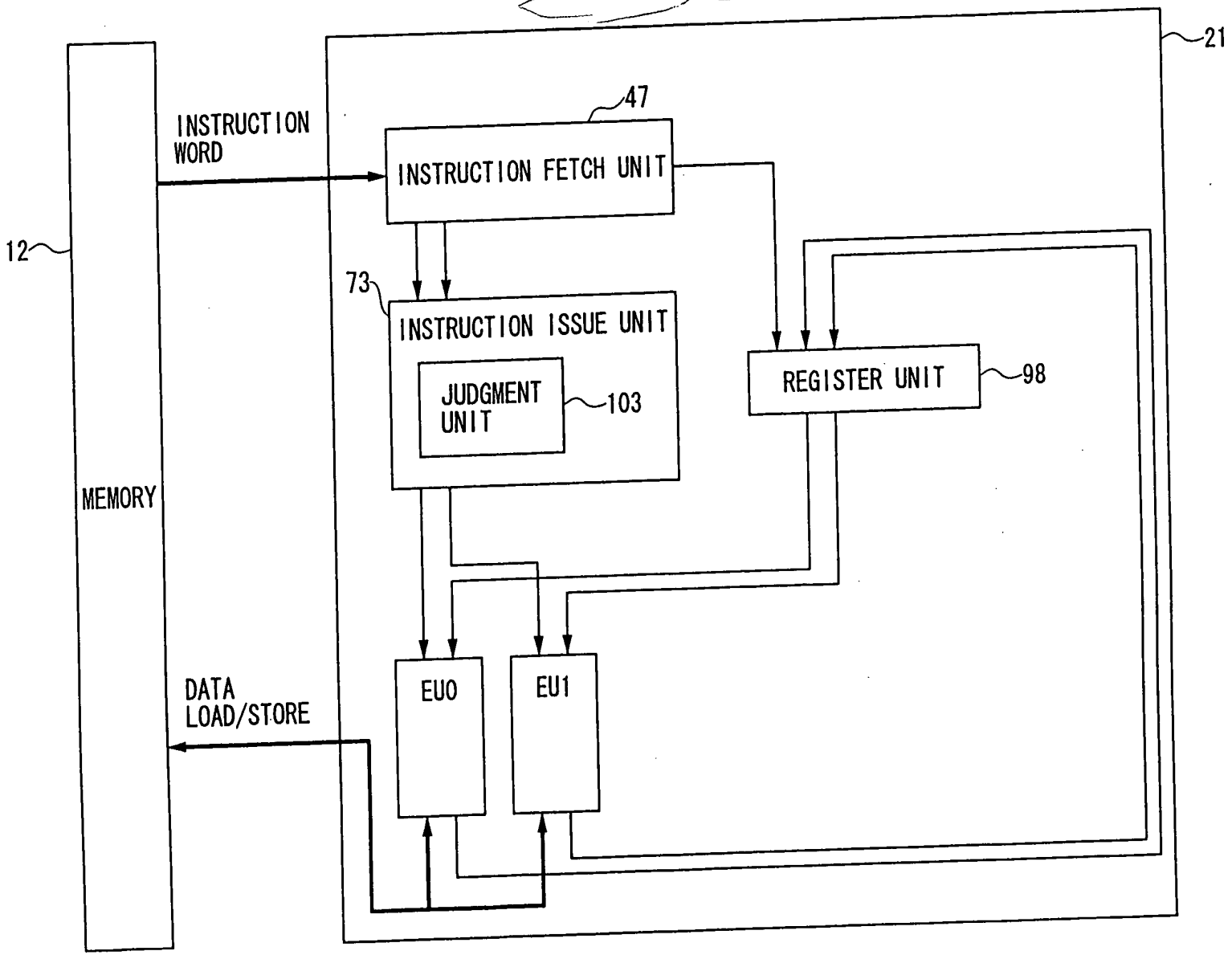
~~[FIG. 5]~~

Formats of instruction words to be supplied to the parallel processor of the first embodiment of the present invention

[FIG. 6]

Structure of a second example of the parallel processor in accordance with the first embodiment of the present invention

FIG.6



~~[FIG. 7]~~

Structure of a first example of a parallel processor in accordance with a second embodiment of the present invention

FIG.7

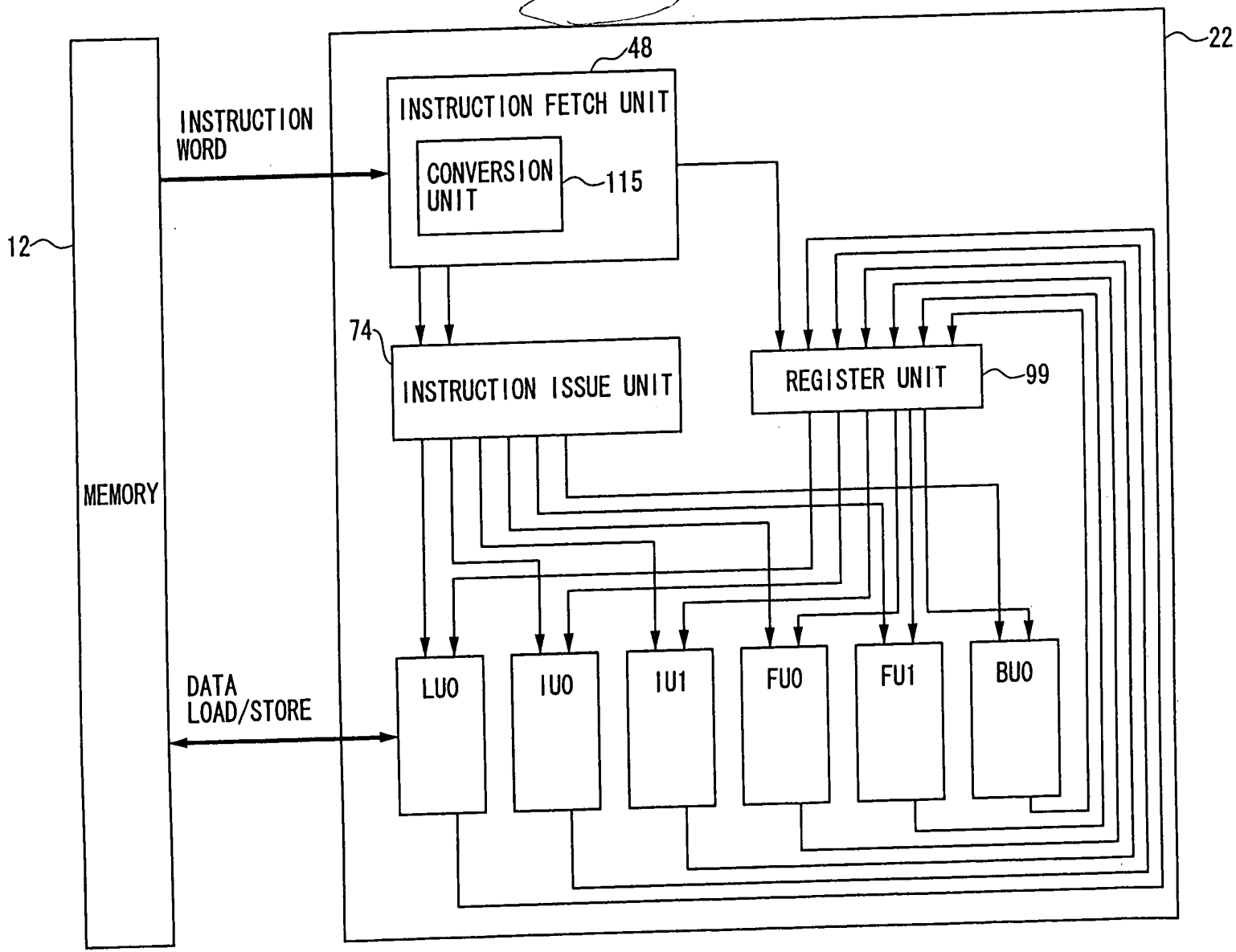
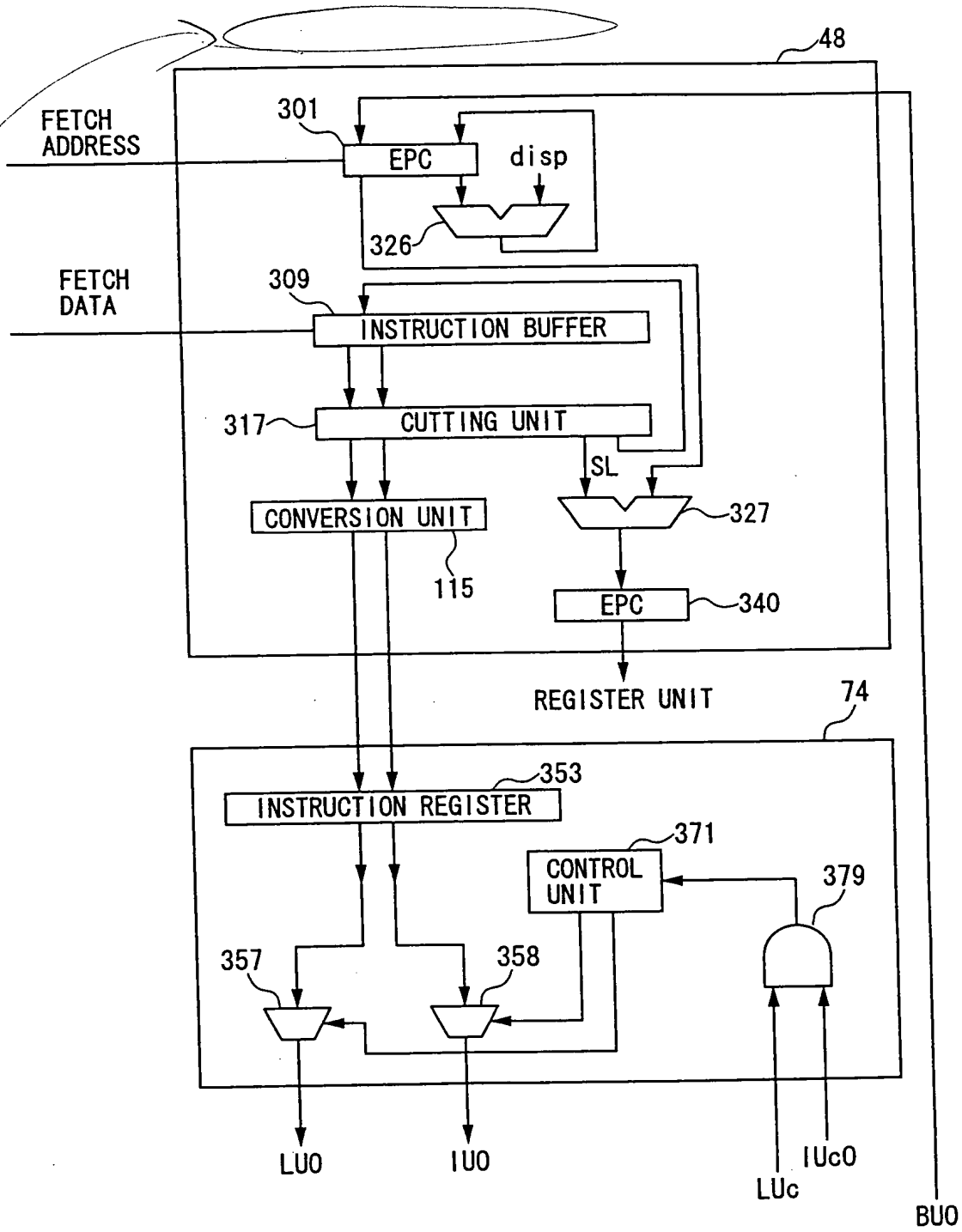


FIG.8



[~~FIG. 8~~]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 7

~~[FIG. 9]~~

FIG. 9

Basic instruction rearrangement in the parallel processor of the second embodiment of the present invention

13

FORMAT OF INSTRUCTION WORDS	LU0		IU0		IU1		FU0		FU1		BU0	
	V	LI	V	II	V	II	V	FI	V	FI	V	BI
0	BI	1	FI	0	—	0	—	0	—	1	FI	0	—	1	BI
0	BI	1	II	0	—	1	II	0	—	0	—	0	—	1	BI
0	BI	1	LI	1	LI	0	—	0	—	0	—	0	—	1	BI
0	FI	1	BI	0	—	0	—	0	—	1	FI	0	—	1	BI
0	FI	1	FI	0	—	0	—	0	—	1	FI	1	FI	0	—
0	FI	1	II	0	—	1	II	0	—	1	FI	0	—	0	—
0	FI	1	LI	1	LI	0	—	0	—	1	FI	0	—	0	—
0	II	1	BI	0	—	1	II	0	—	0	—	0	—	1	BI
0	II	1	FI	0	—	1	II	0	—	1	FI	0	—	0	—
0	II	1	II	0	—	1	II	1	II	0	—	0	—	0	—
0	II	1	LI	1	LI	1	II	0	—	0	—	0	—	0	—
0	LI	1	BI	1	LI	0	—	0	—	0	—	0	—	1	BI
0	LI	1	FI	1	LI	0	—	0	—	1	FI	0	—	0	—
0	LI	1	II	1	LI	1	II	0	—	0	—	0	—	0	—
1	BI			0	—	0	—	0	—	0	—	0	—	1	BI
1	FI			0	—	0	—	0	—	1	FI	0	—	0	—
1	II			0	—	1	II	0	—	0	—	0	—	0	—
1	LI			1	LI	0	—	0	—	0	—	0	—	0	—

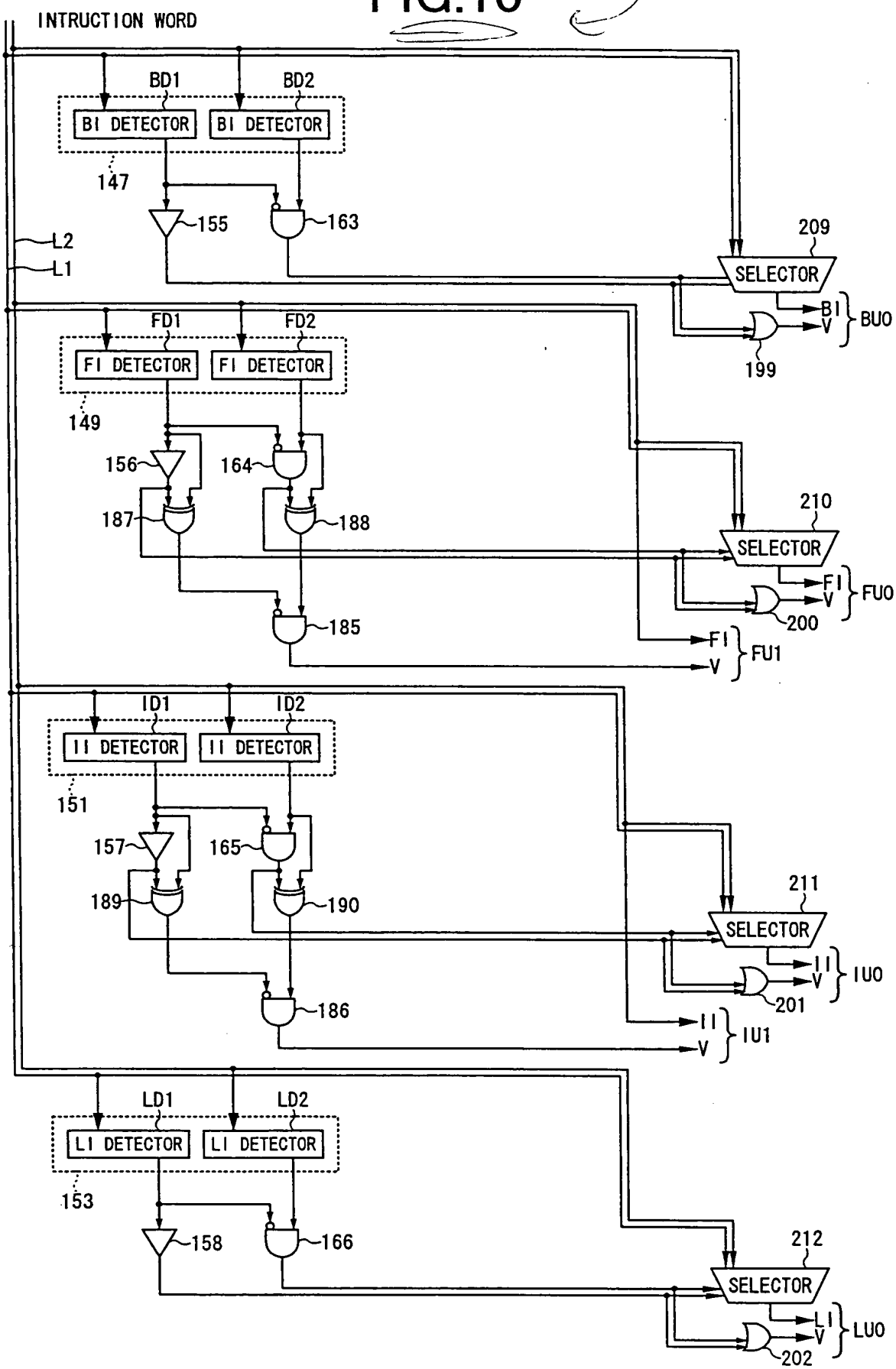
15

17

[~~FIG. 10~~]

Circuit diagram of a conversion unit in the parallel processor shown in FIG. 7

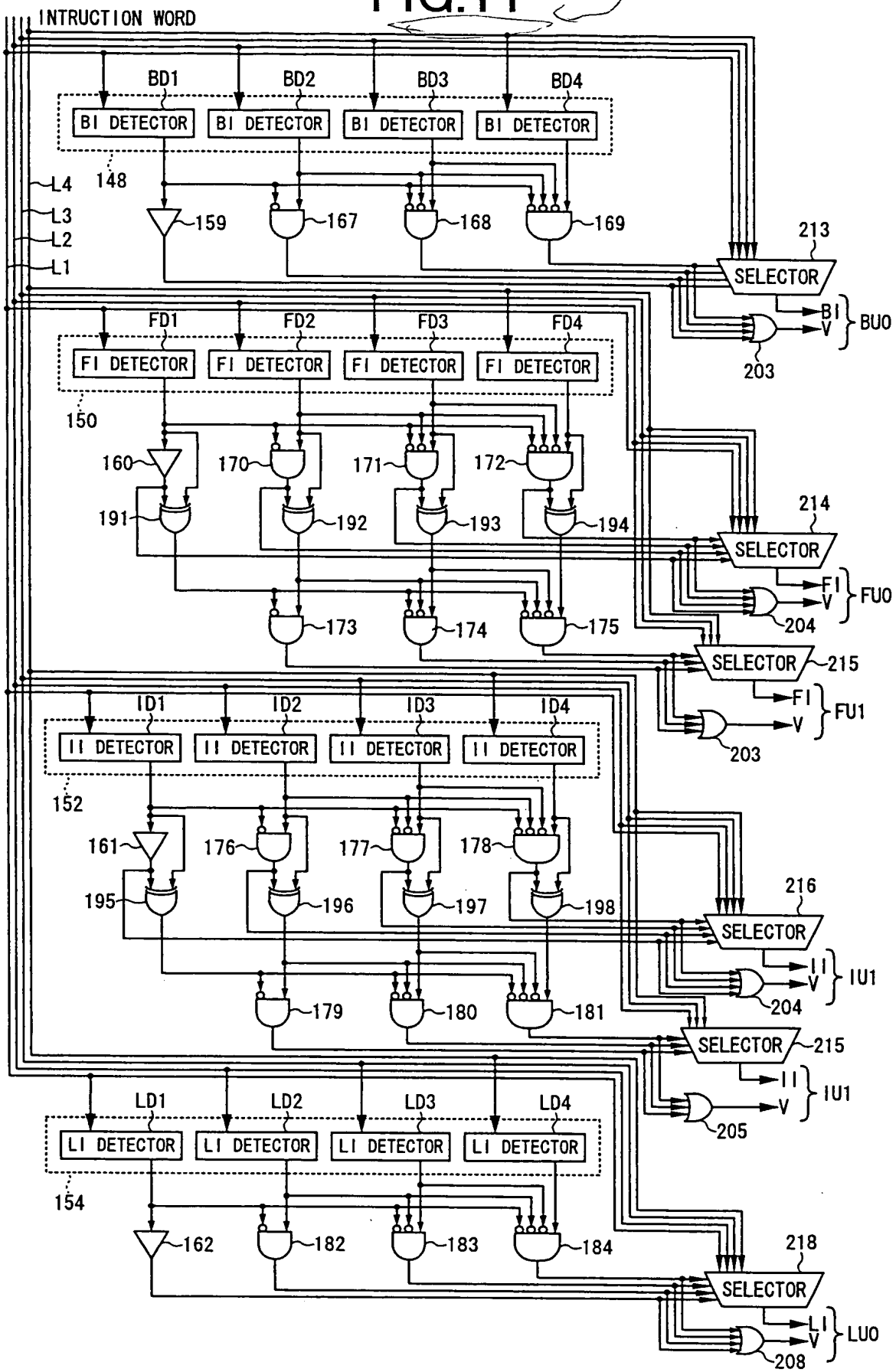
FIG.10



[FIG. 11]

Circuit diagram of the conversion unit in a case where the maximum basic instruction word length is 4

FIG.11



[~~FIG. 12~~]

Structure of a second example of the parallel processor in accordance with the second embodiment of the present invention

FIG.12

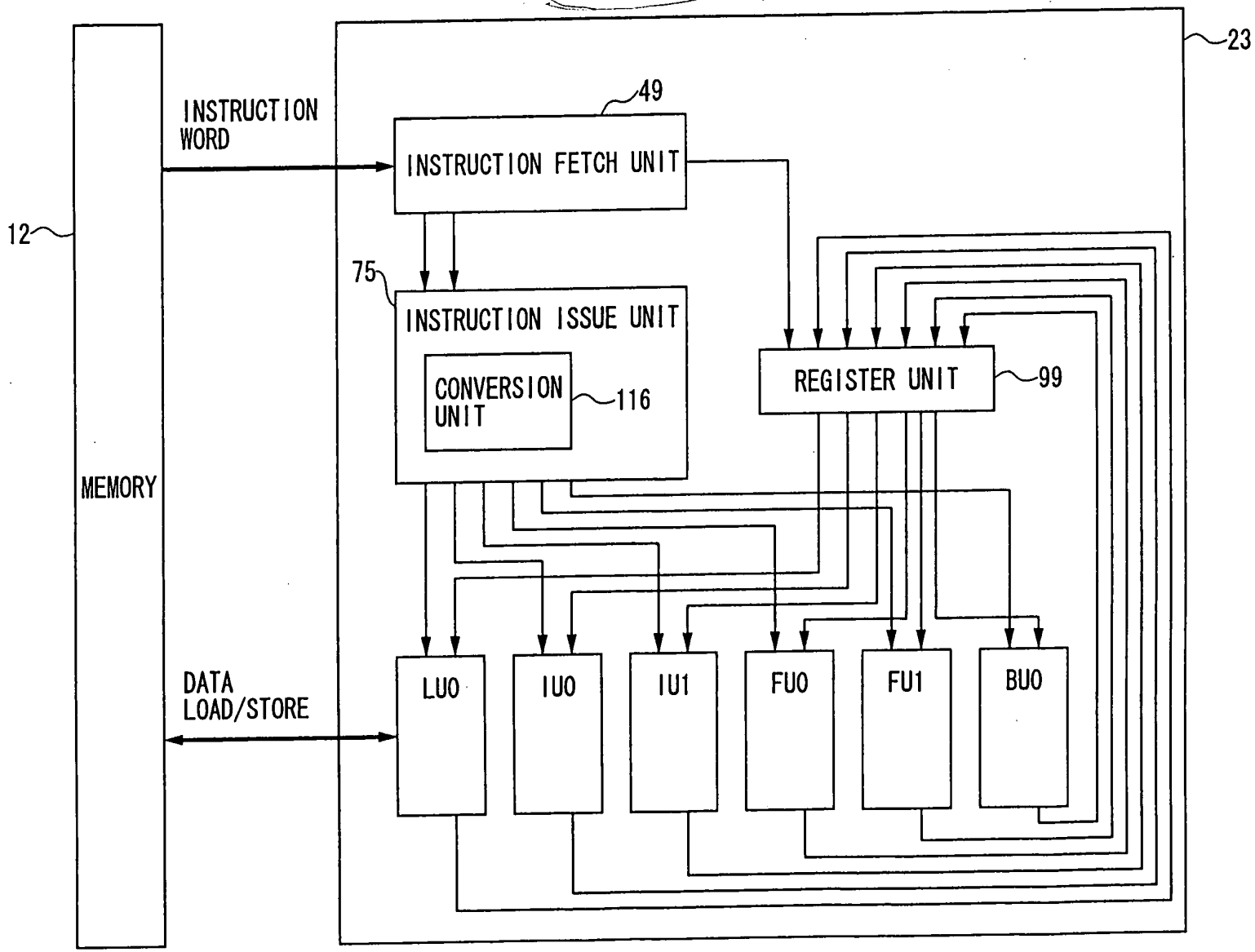
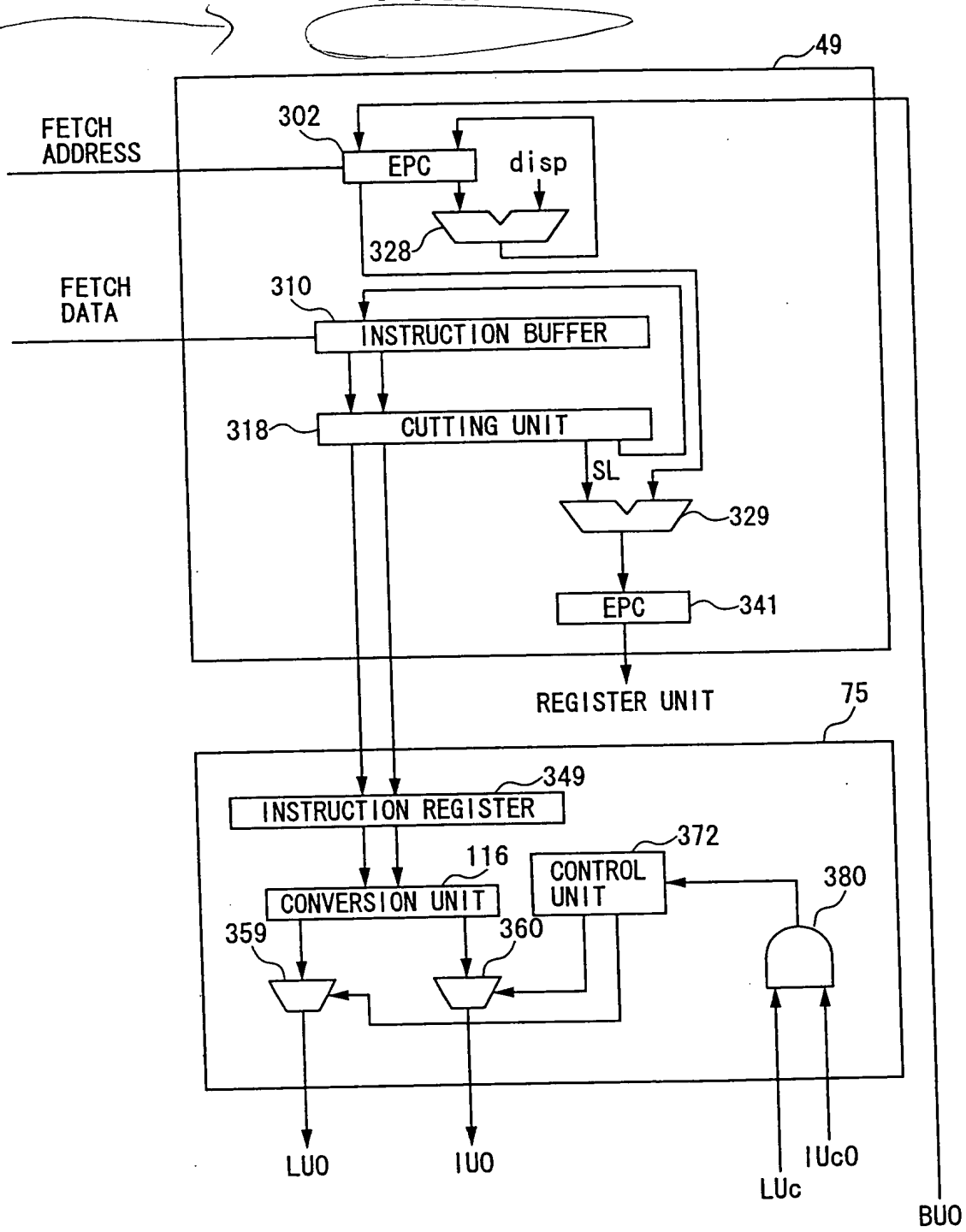


FIG.13



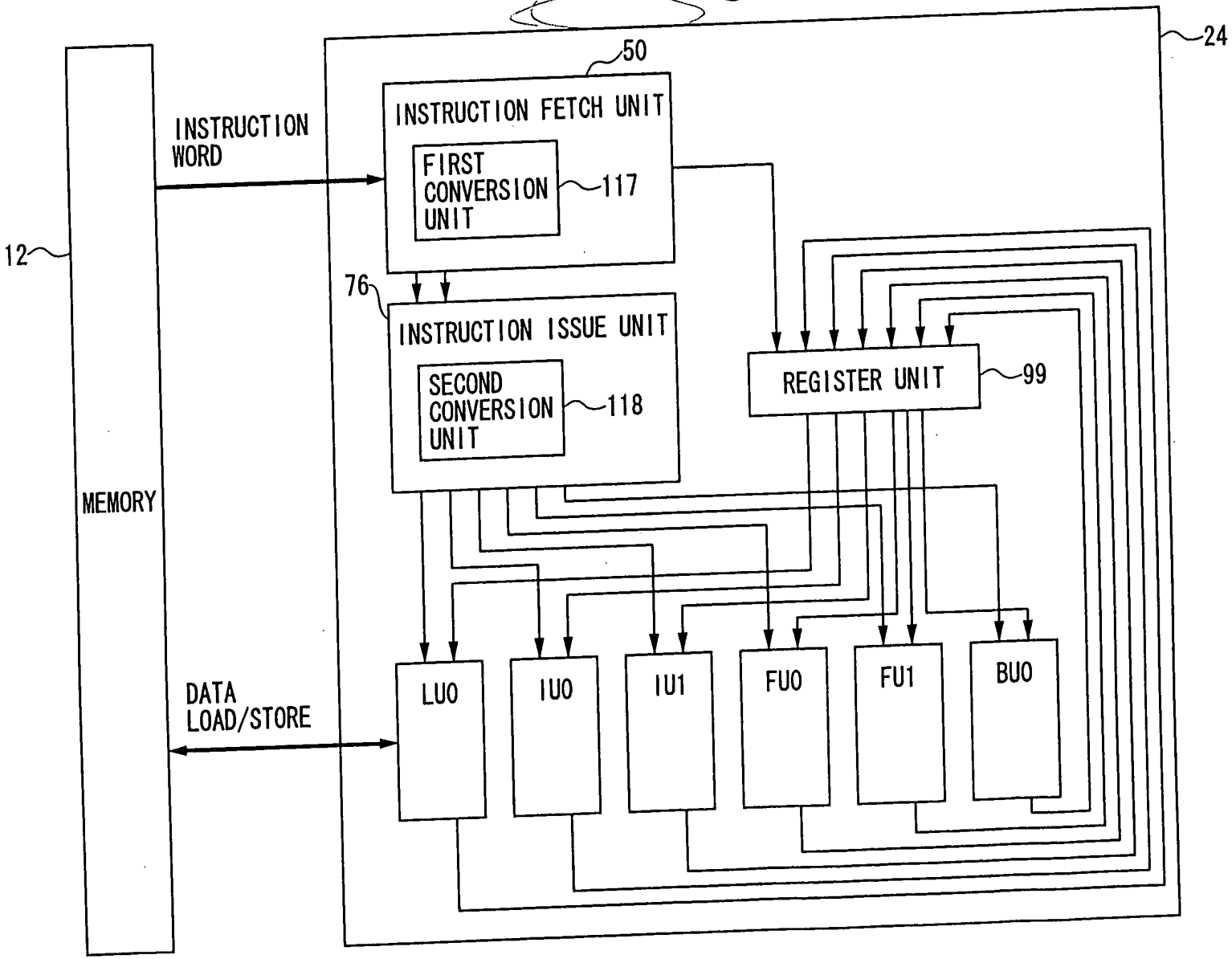
[~~FIG. 13~~]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 12

[FIG. 14]

Structure of a third example of the parallel processor in accordance with the second embodiment of the present invention

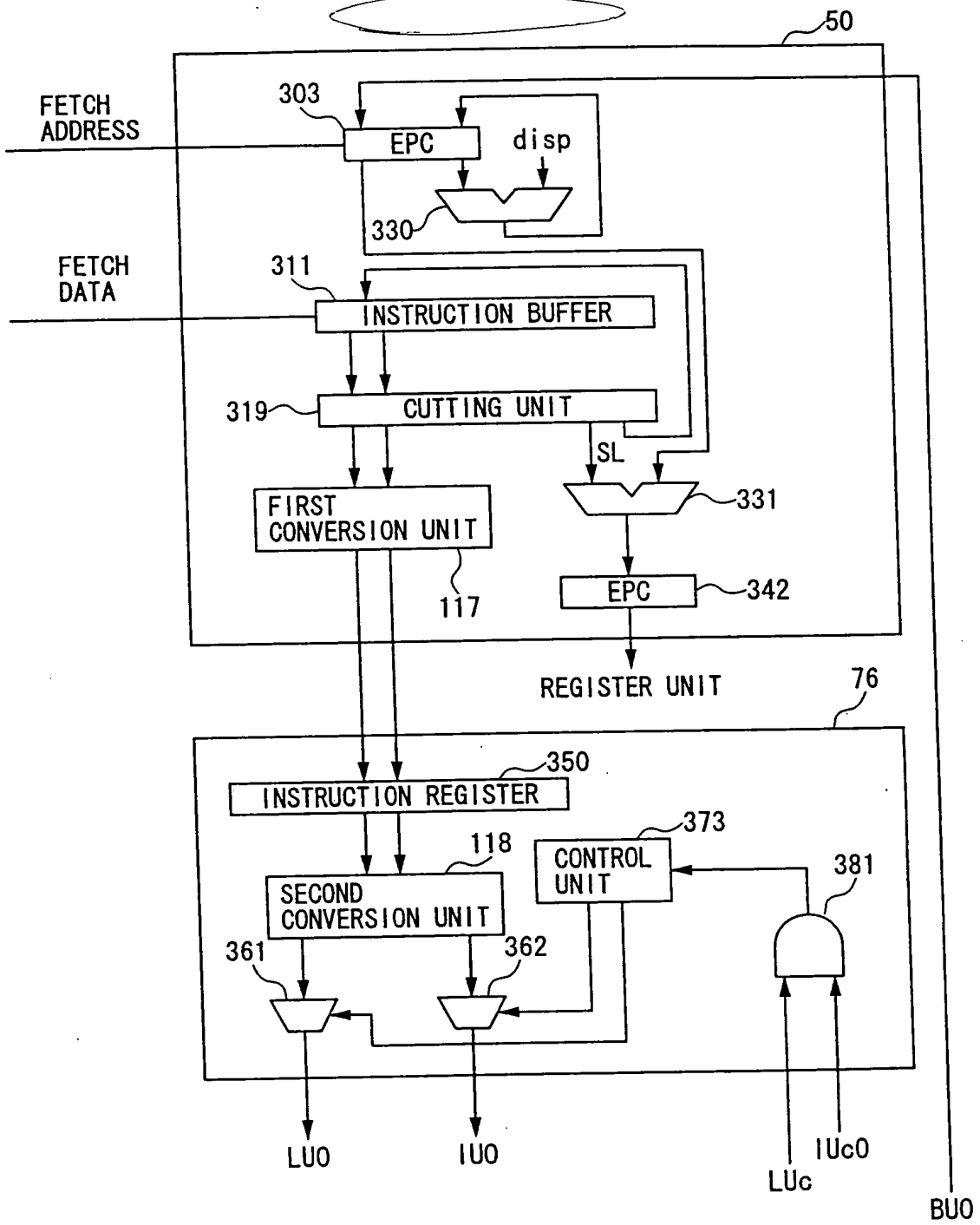
FIG.14



[FIG. 15]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 14

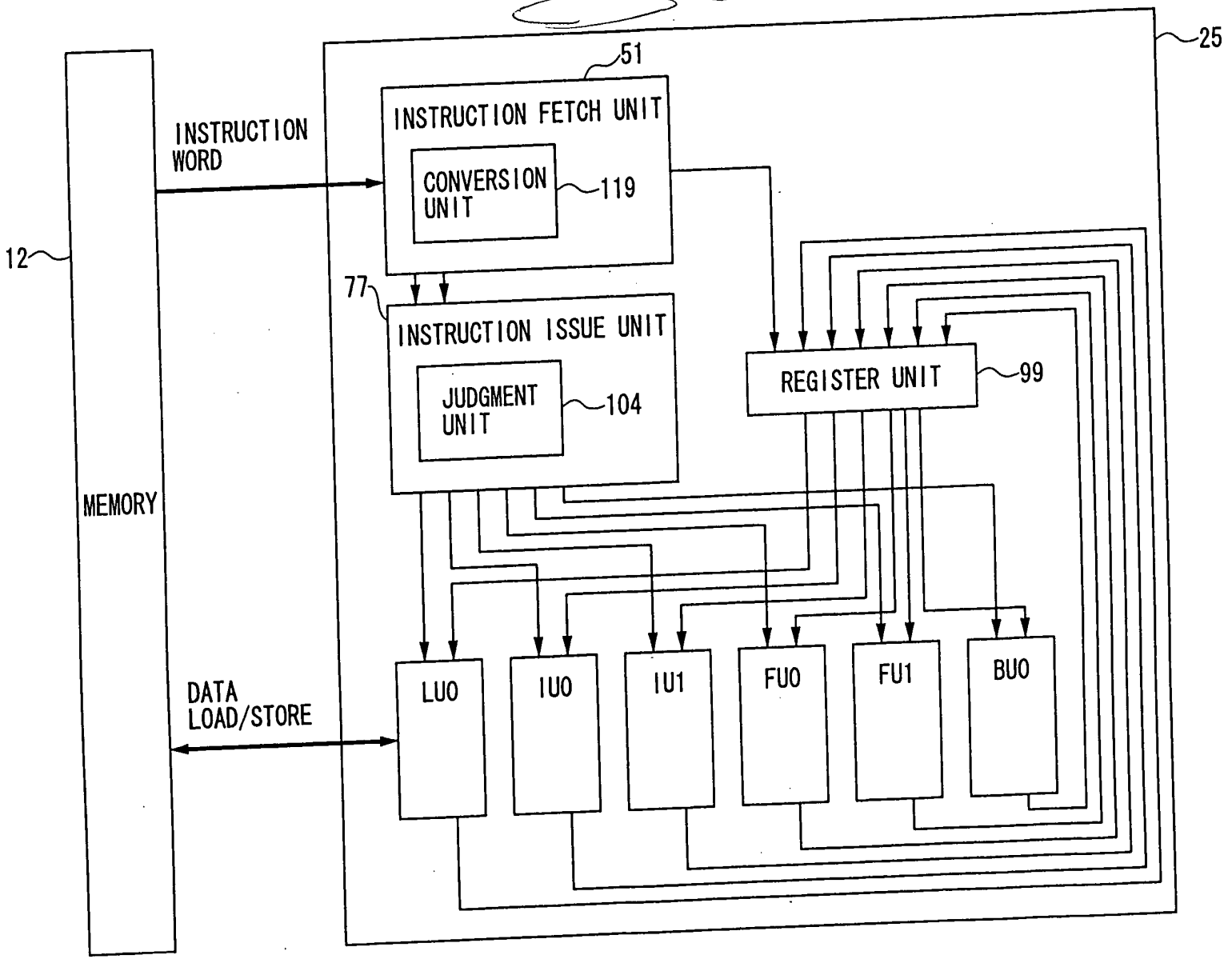
FIG.15



[FIG. 16]

Structure of a fourth example of the parallel processor in accordance with the second embodiment of the present invention

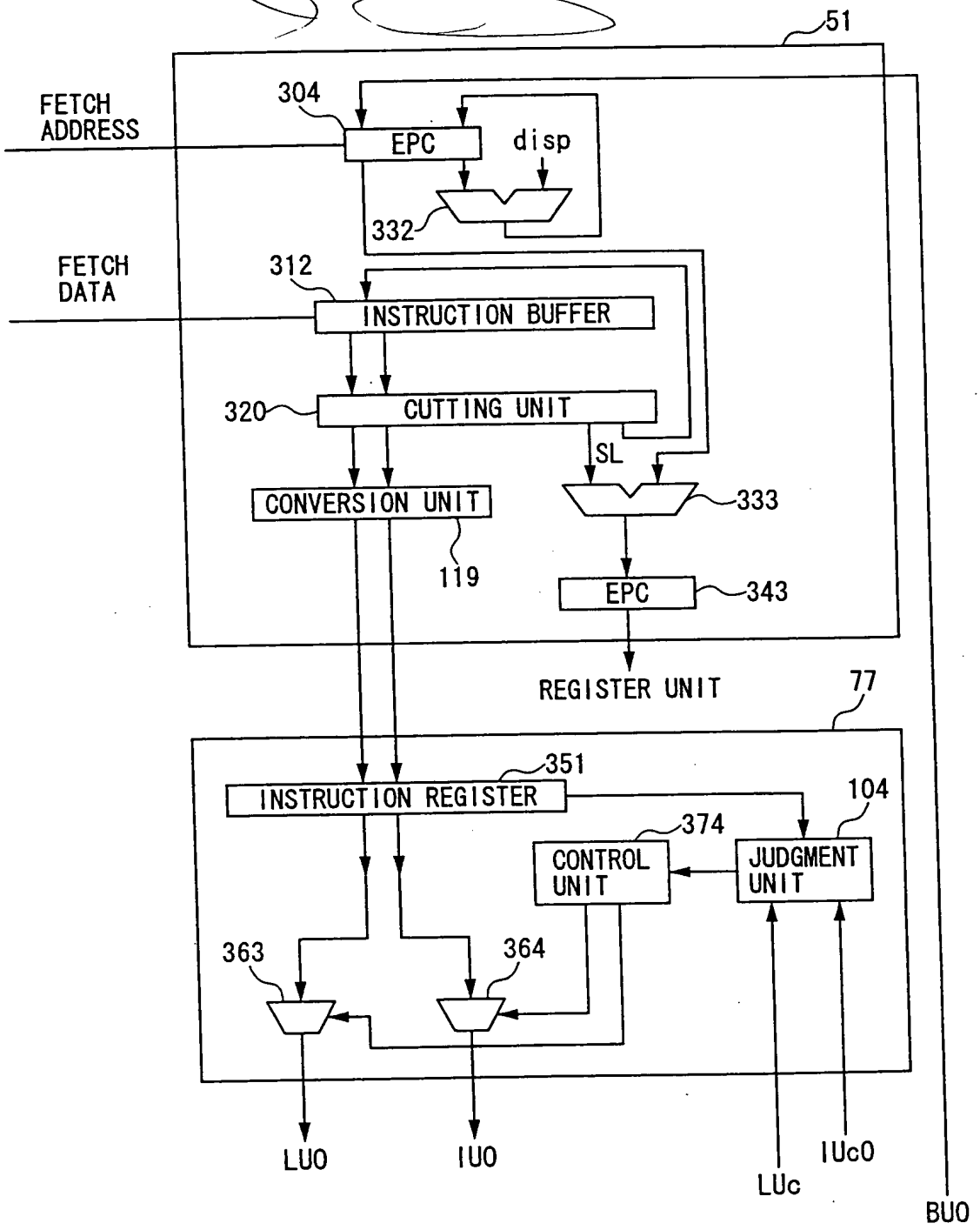
FIG.16



~~[FIG. 17]~~

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 16

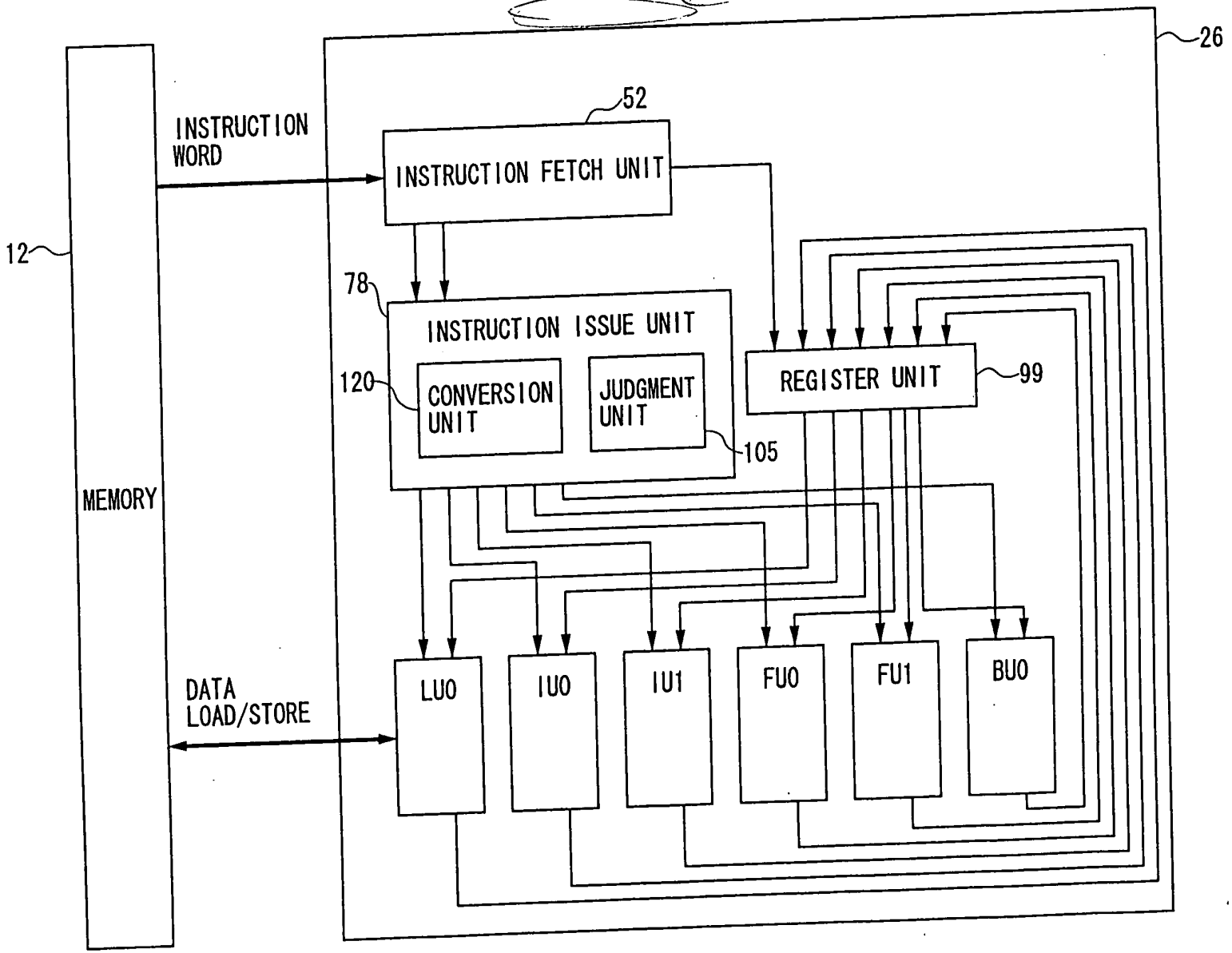
FIG.17



[~~FIG. 18~~]

Structure of a fifth example of the parallel processor in accordance with the second embodiment of the present invention

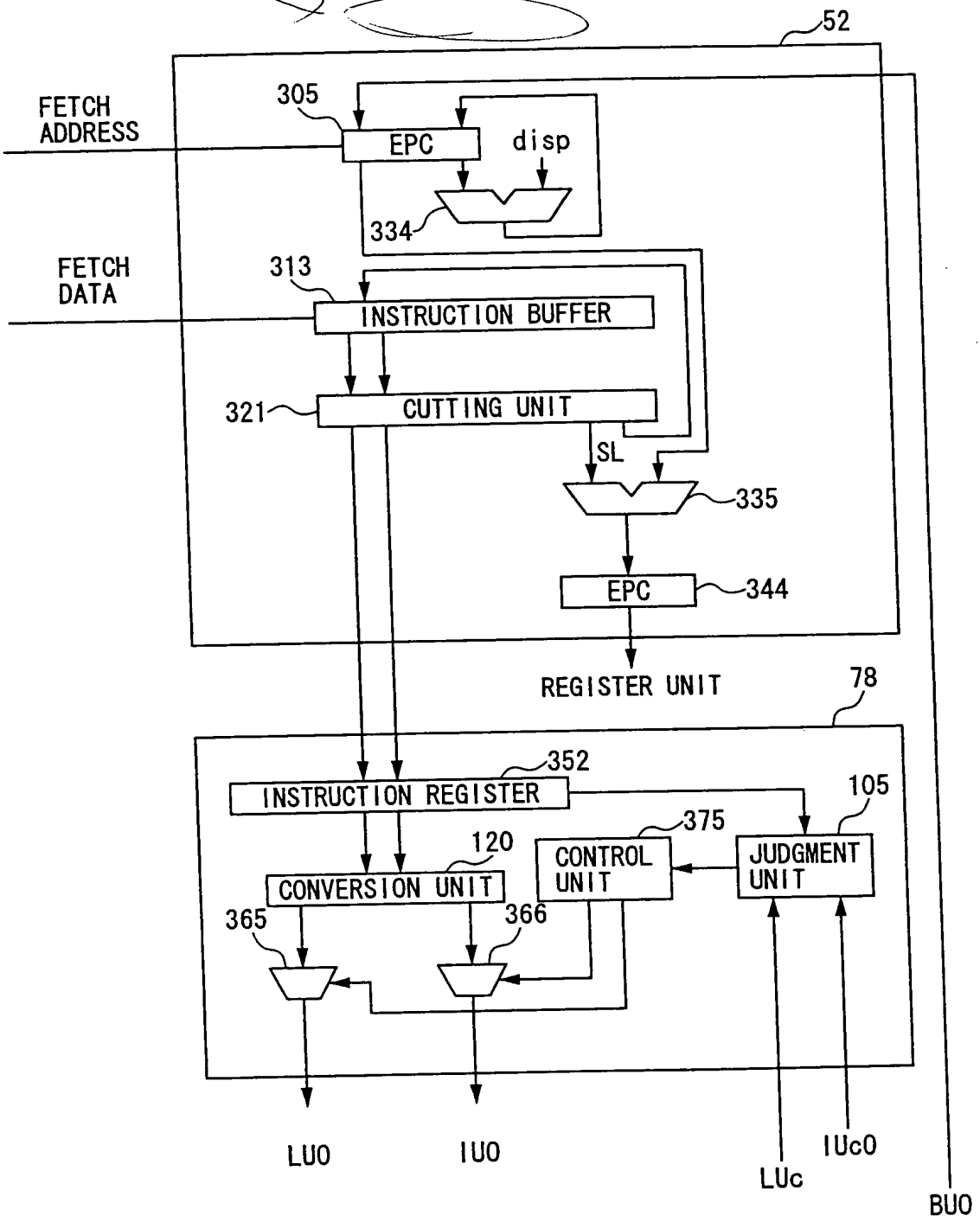
FIG.18



[~~FIG. 19~~]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 18

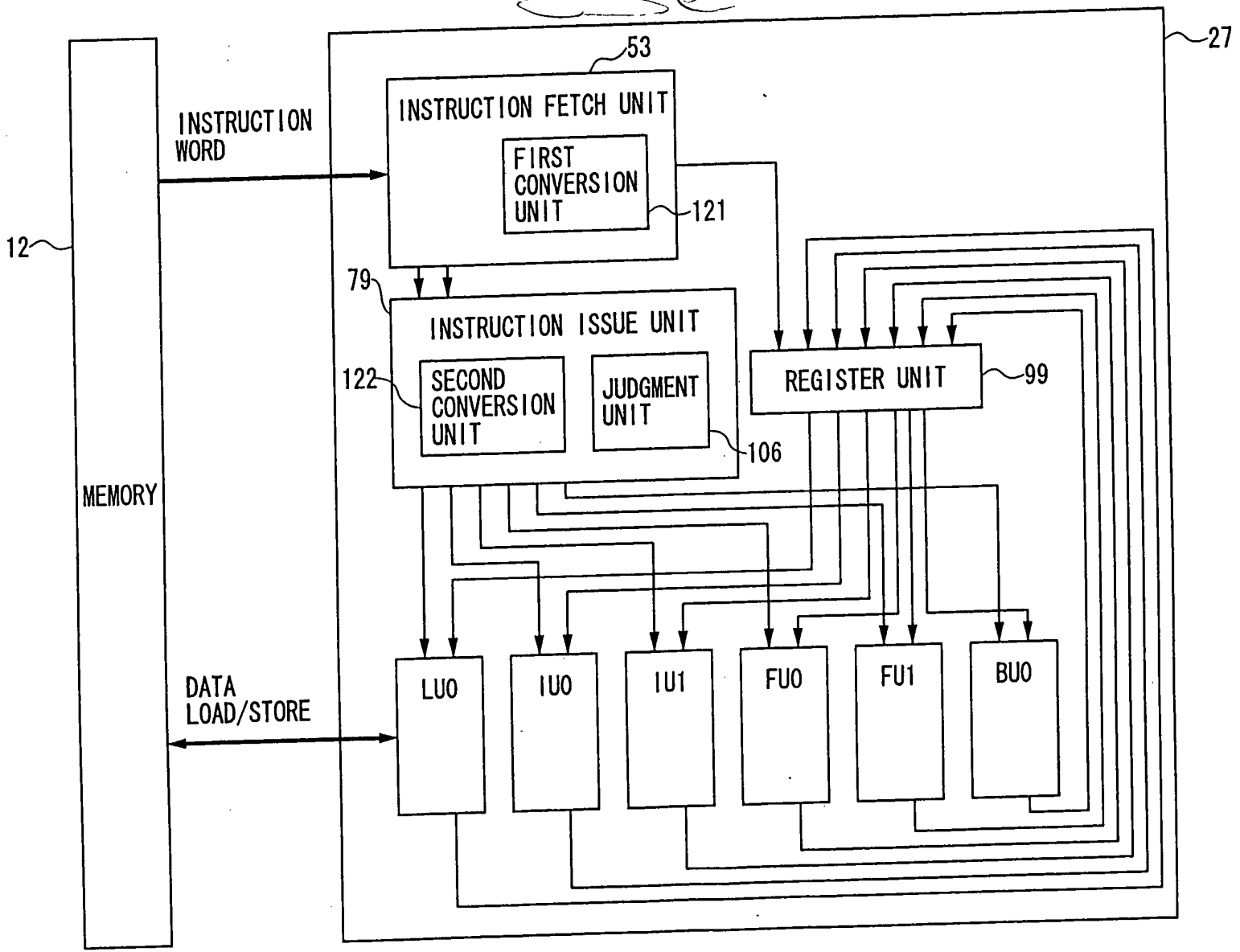
FIG.19



[FIG. 20]

Structure of a sixth example of the parallel processor in accordance with the second embodiment of the present invention

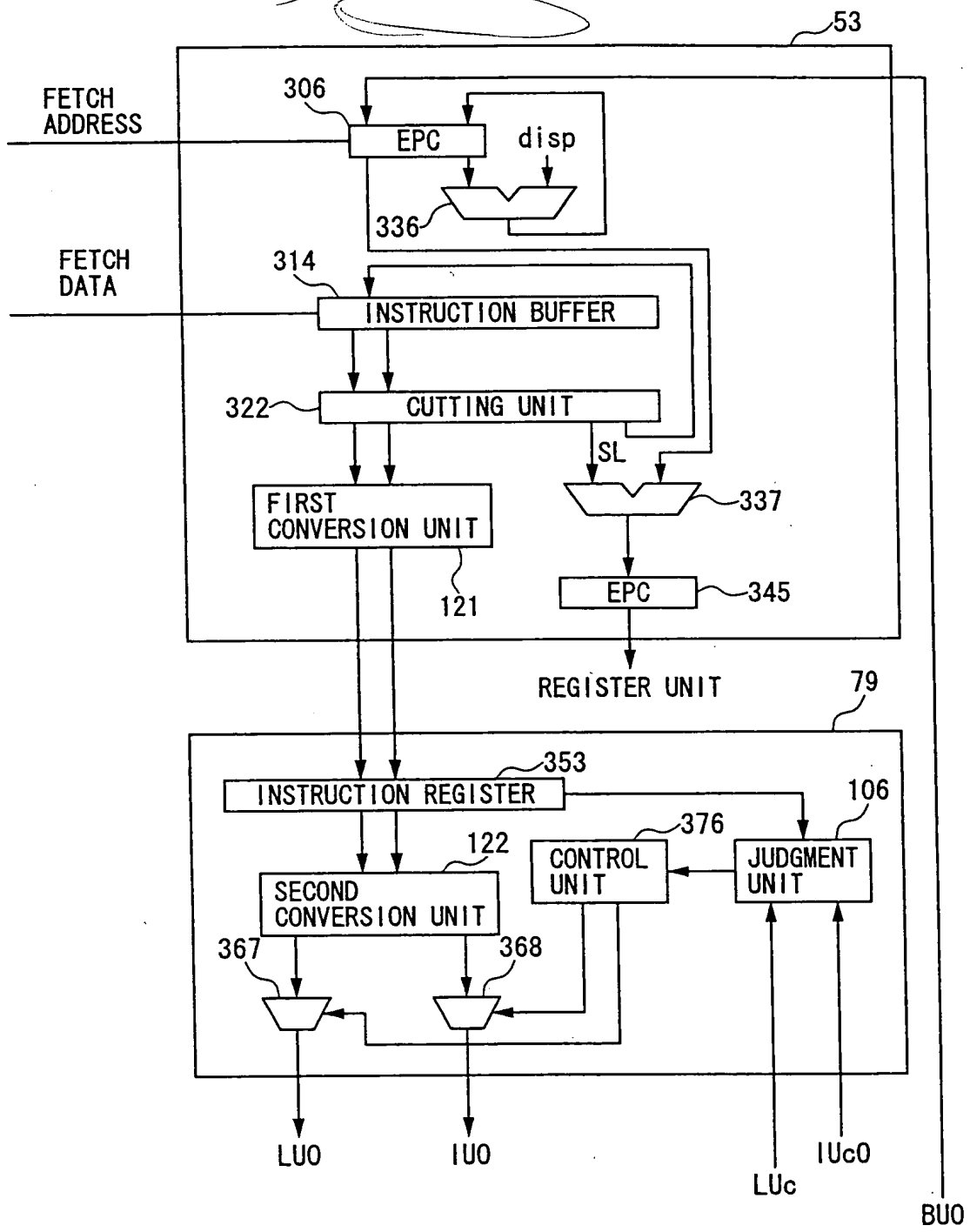
FIG.20



[FIG. 21]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 20

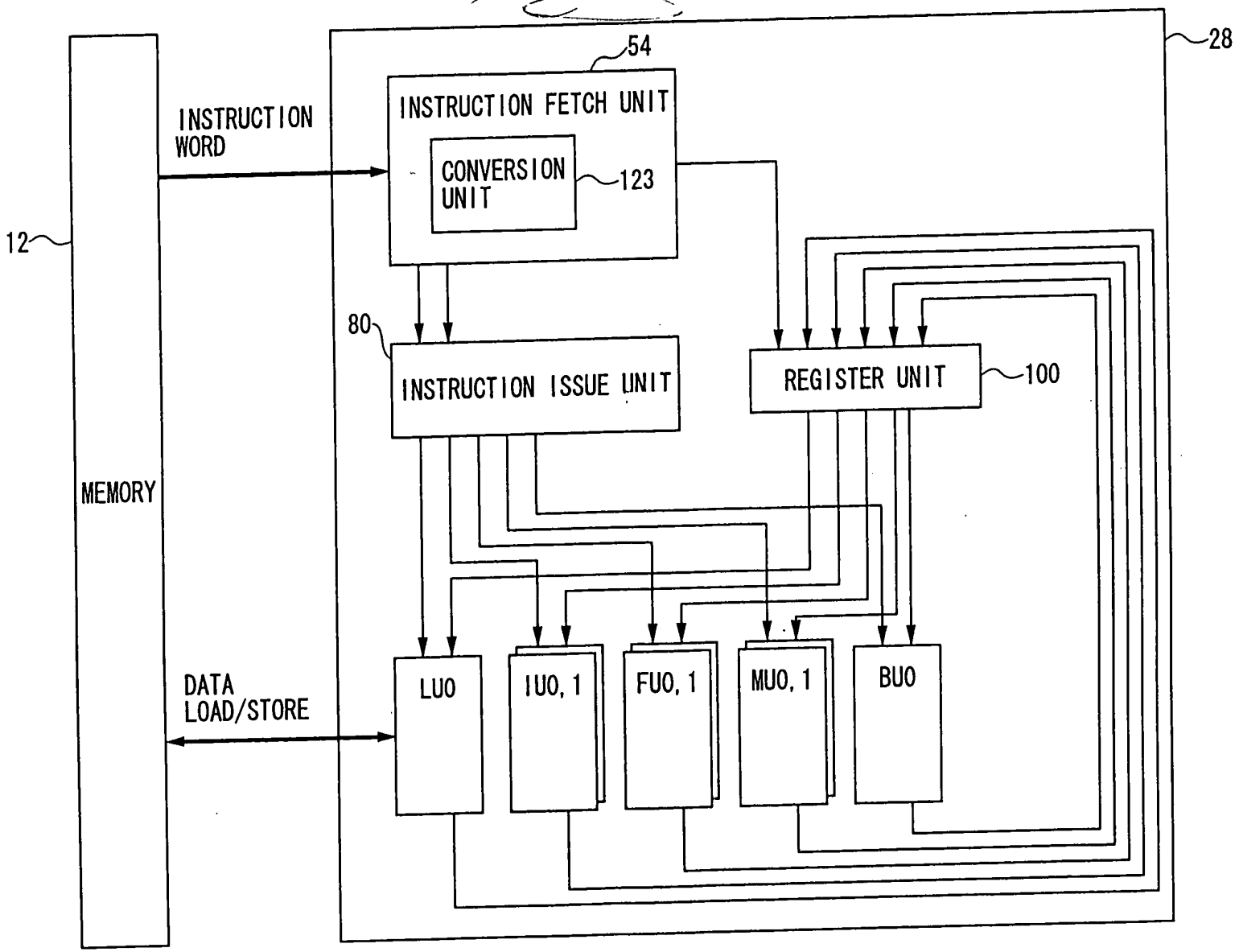
FIG.21



~~[FIG. 22]~~

Structure of a first example of a parallel processor in accordance with a third embodiment of the present invention;

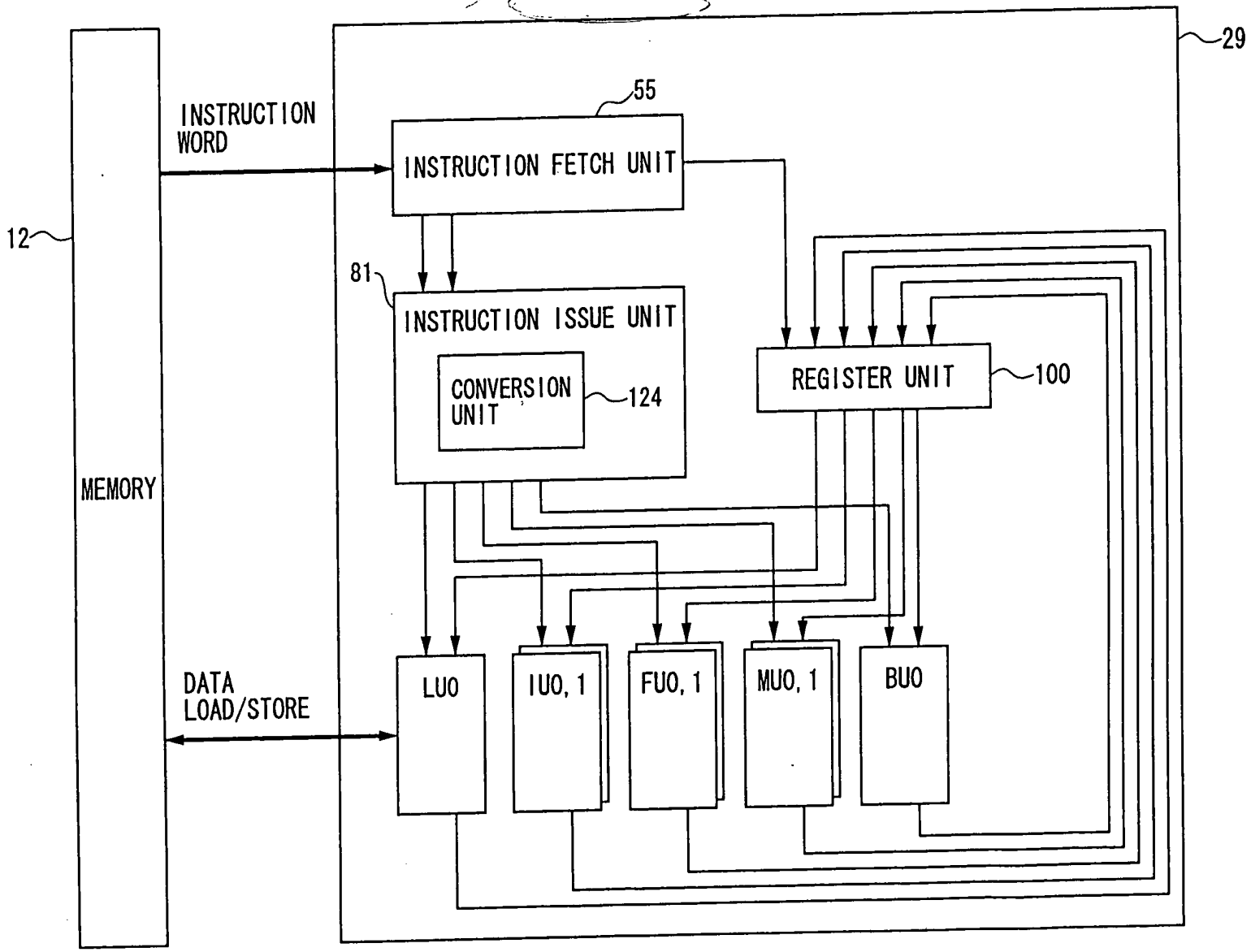
FIG.22



[FIG. 23]

Structure of a second example of the parallel processor in accordance with the third embodiment of the present invention

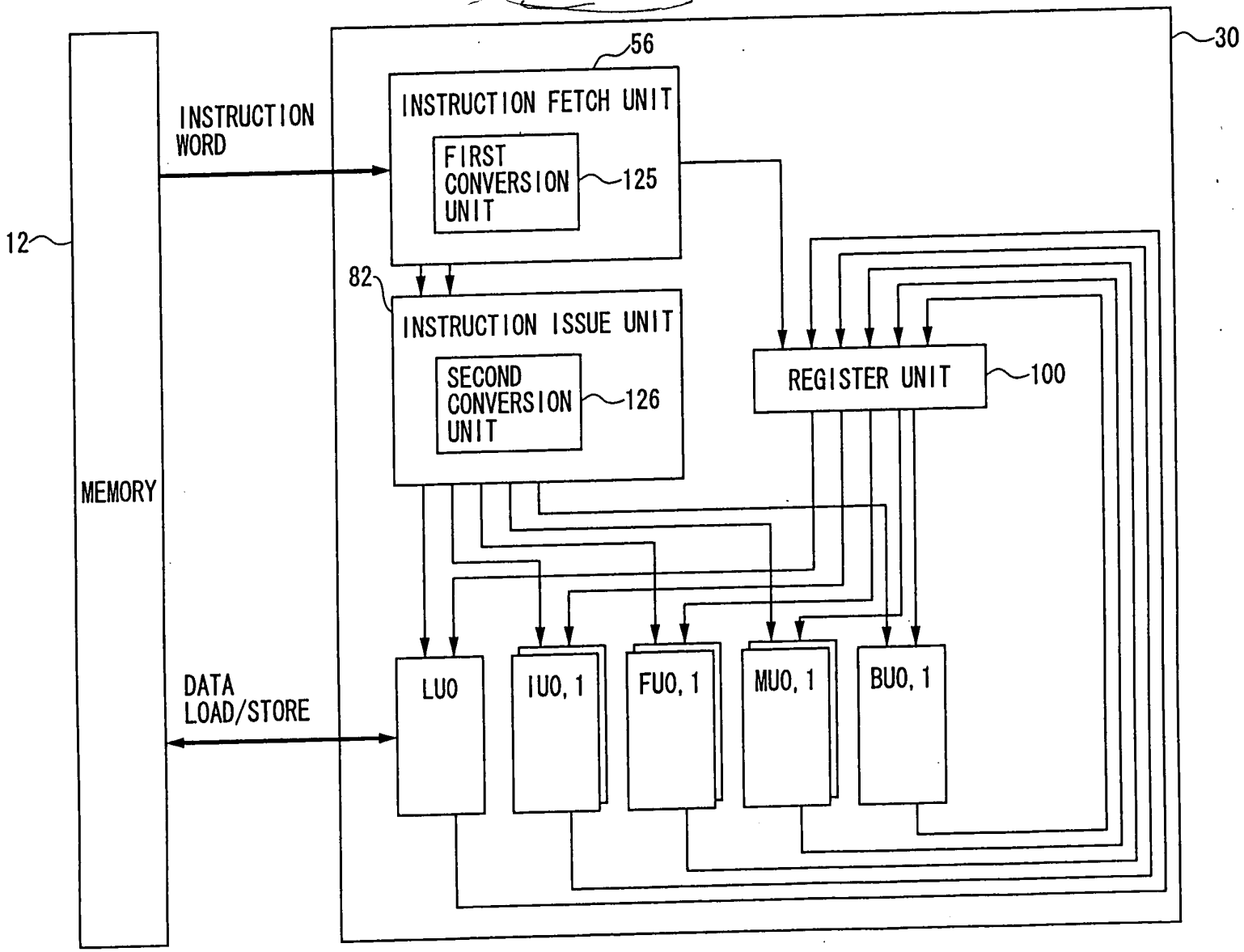
FIG.23



~~FIG. 24~~

Structure of a third example of the parallel processor in accordance with the third embodiment of the present invention

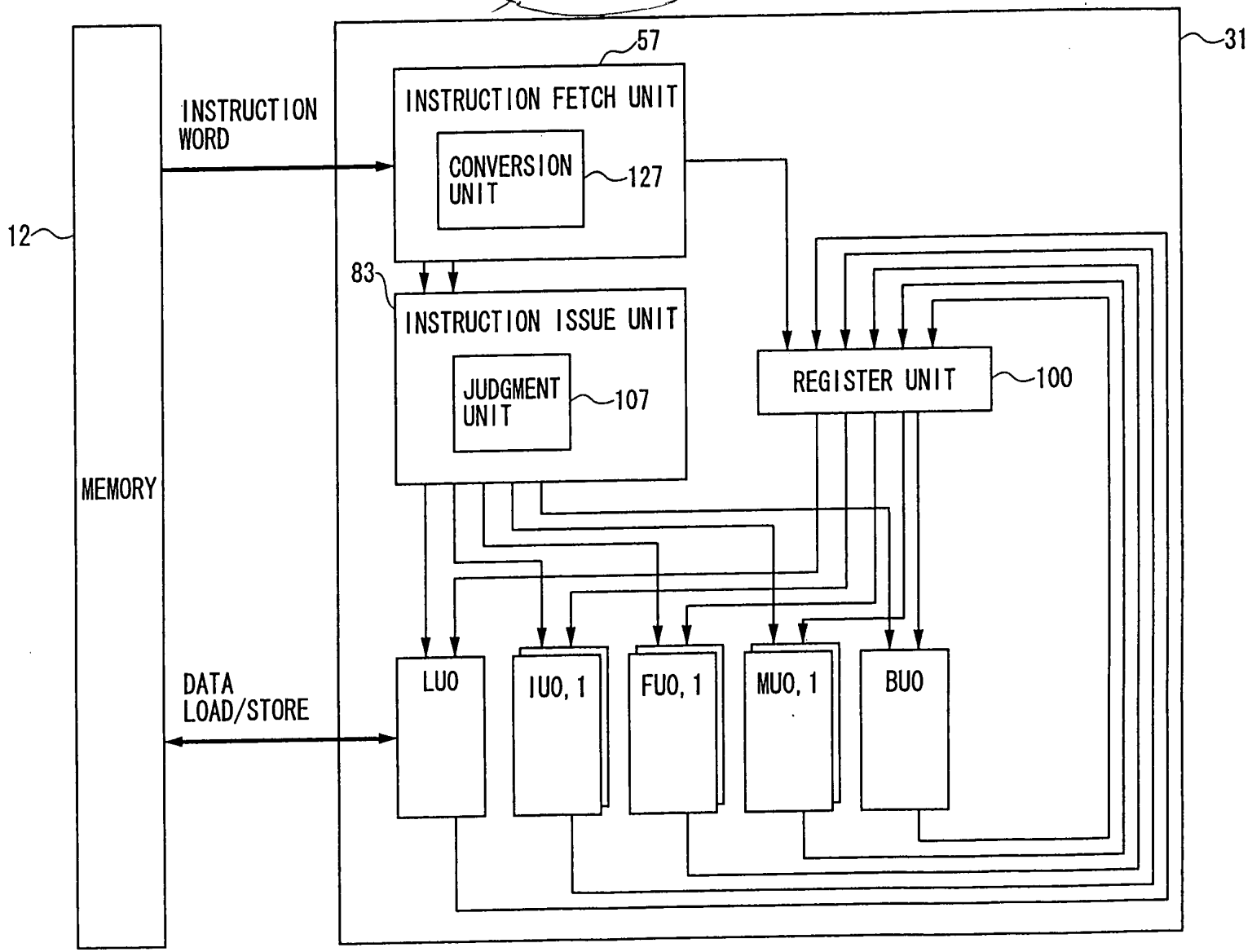
FIG.24



~~[FIG. 25]~~

Structure of a fourth example of the parallel processor in accordance with the third embodiment of the present invention

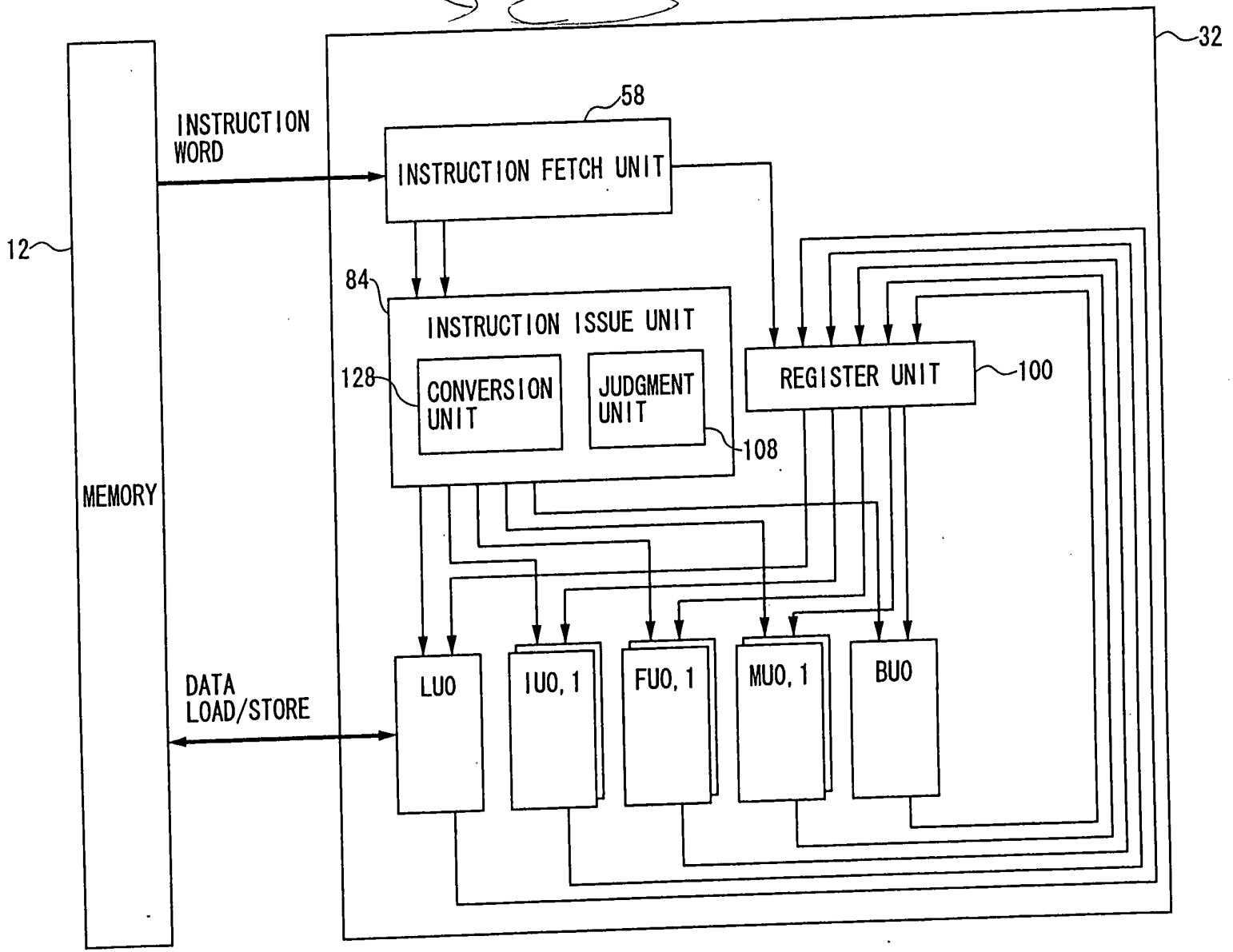
FIG.25



[~~FIG. 26~~]

Structure of a fifth example of the parallel processor in accordance with the third embodiment of the present invention

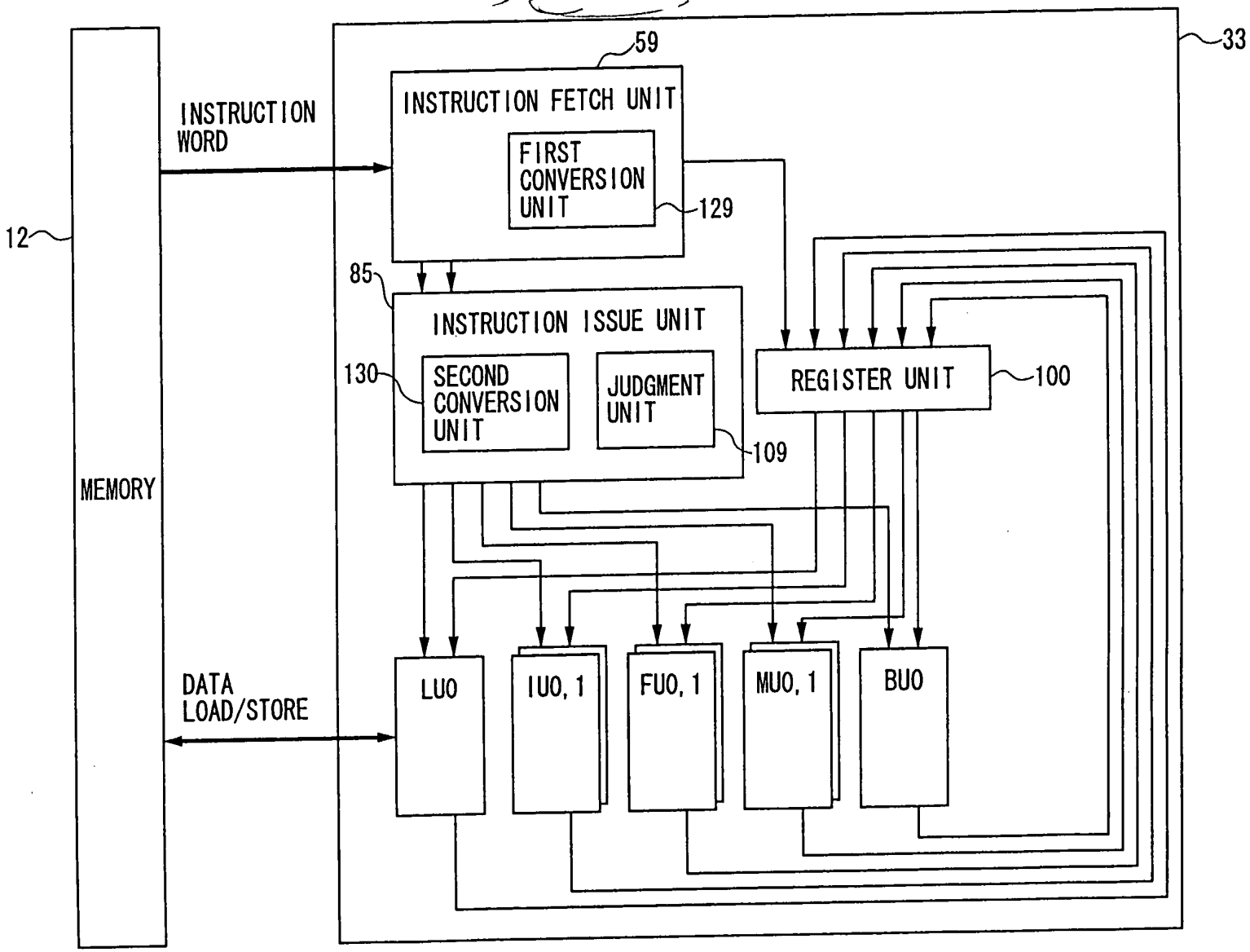
FIG.26



[FIG. 27]

Structure of a sixth example of the parallel processor in accordance with the third embodiment of the present invention

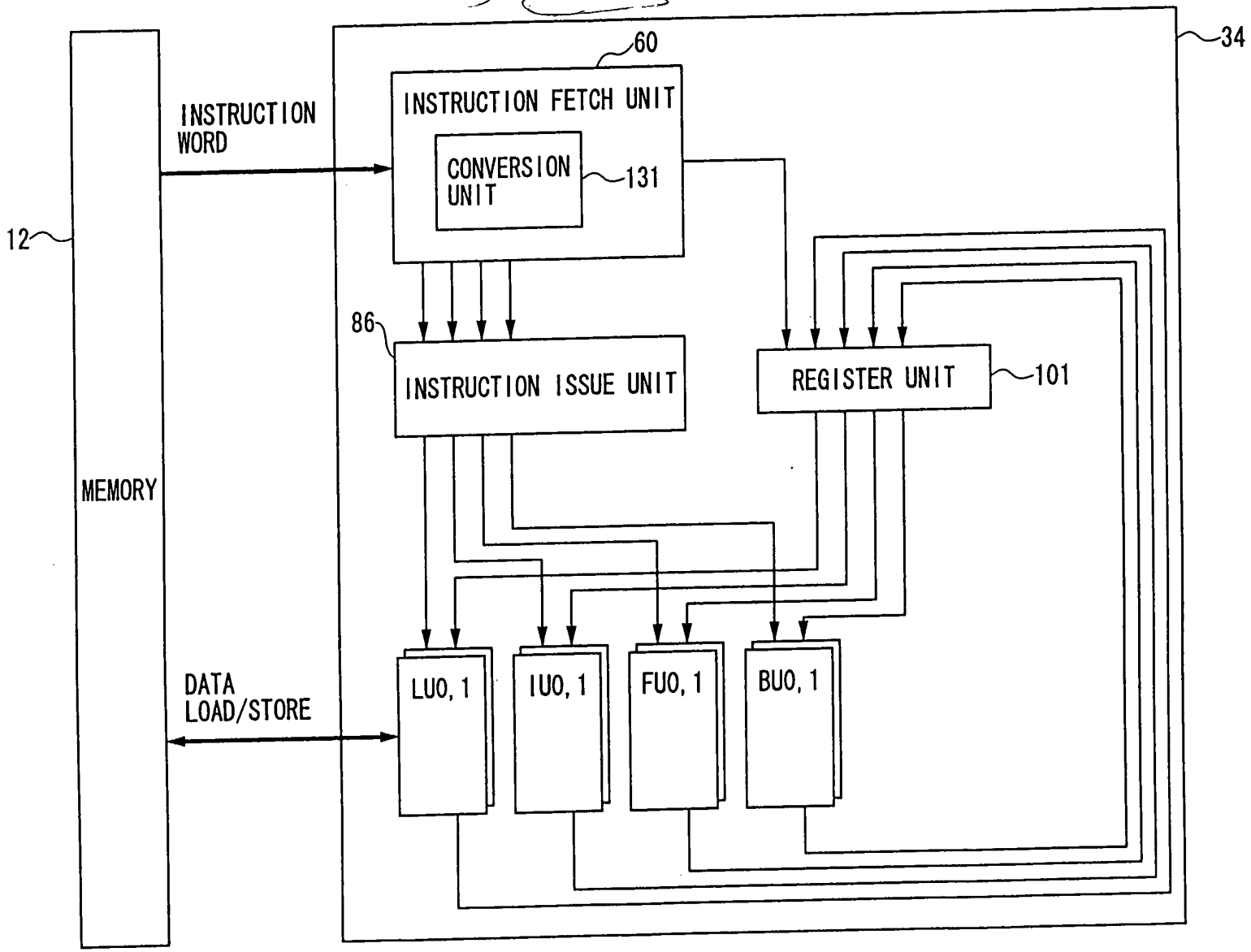
FIG.27



[~~FIG. 28~~]

Structure of a first example of a parallel processor in accordance with a fourth embodiment of the present invention

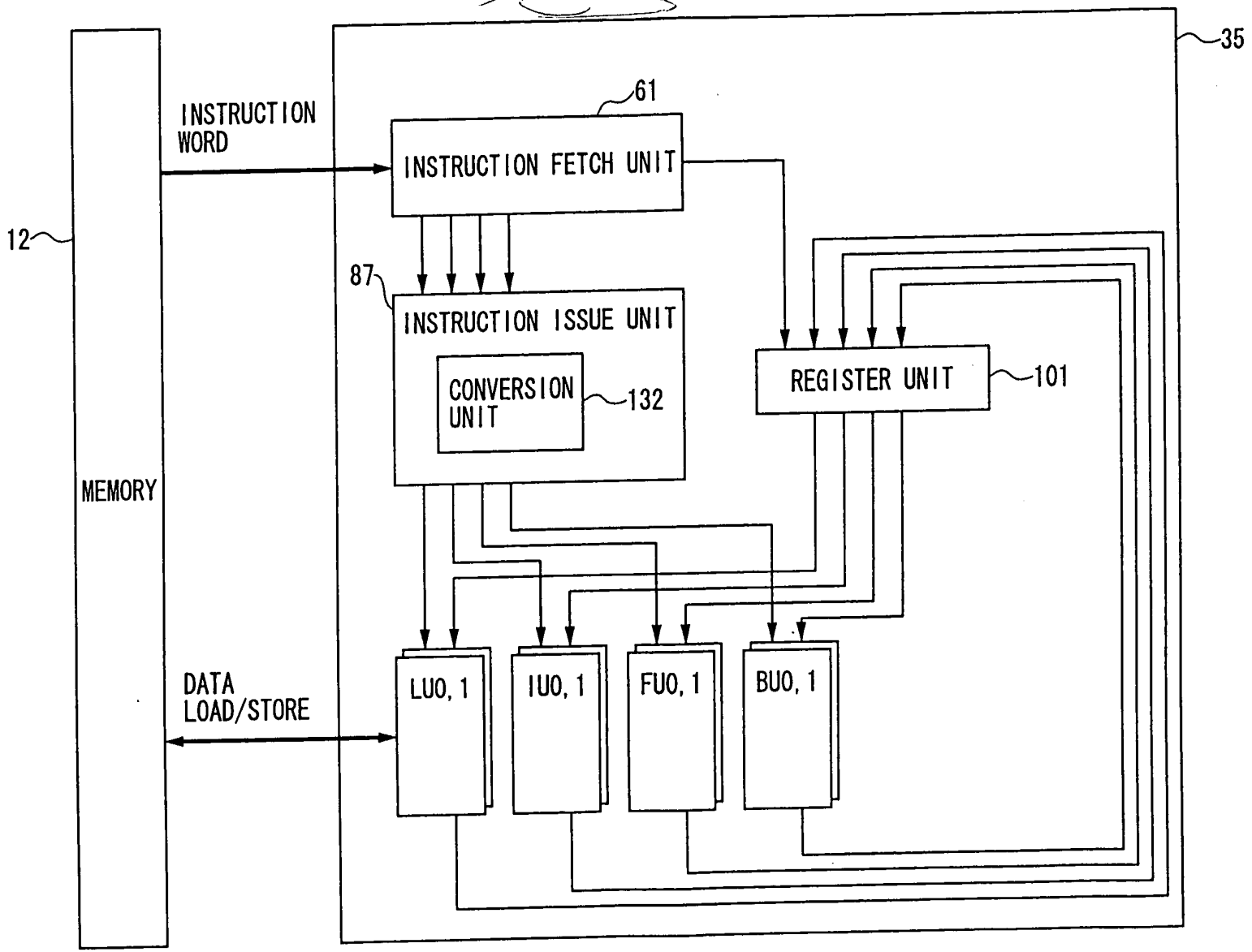
FIG.28



[~~FIG. 29~~]

Structure of a second example of the parallel processor in accordance with the fourth embodiment of the present invention

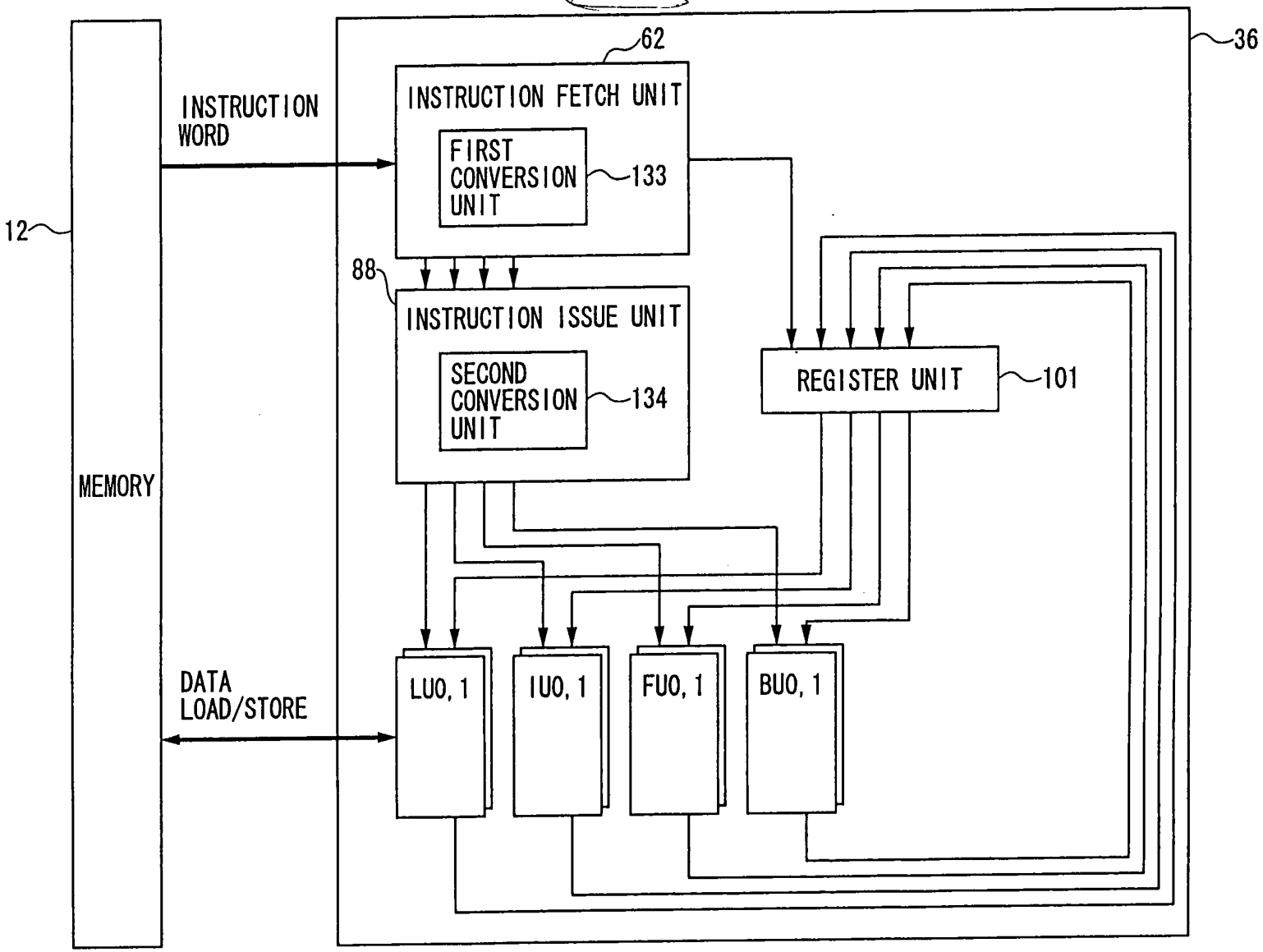
FIG.29



[FIG. 30]

Structure of a third example of the parallel processor in accordance with the fourth embodiment of the present invention

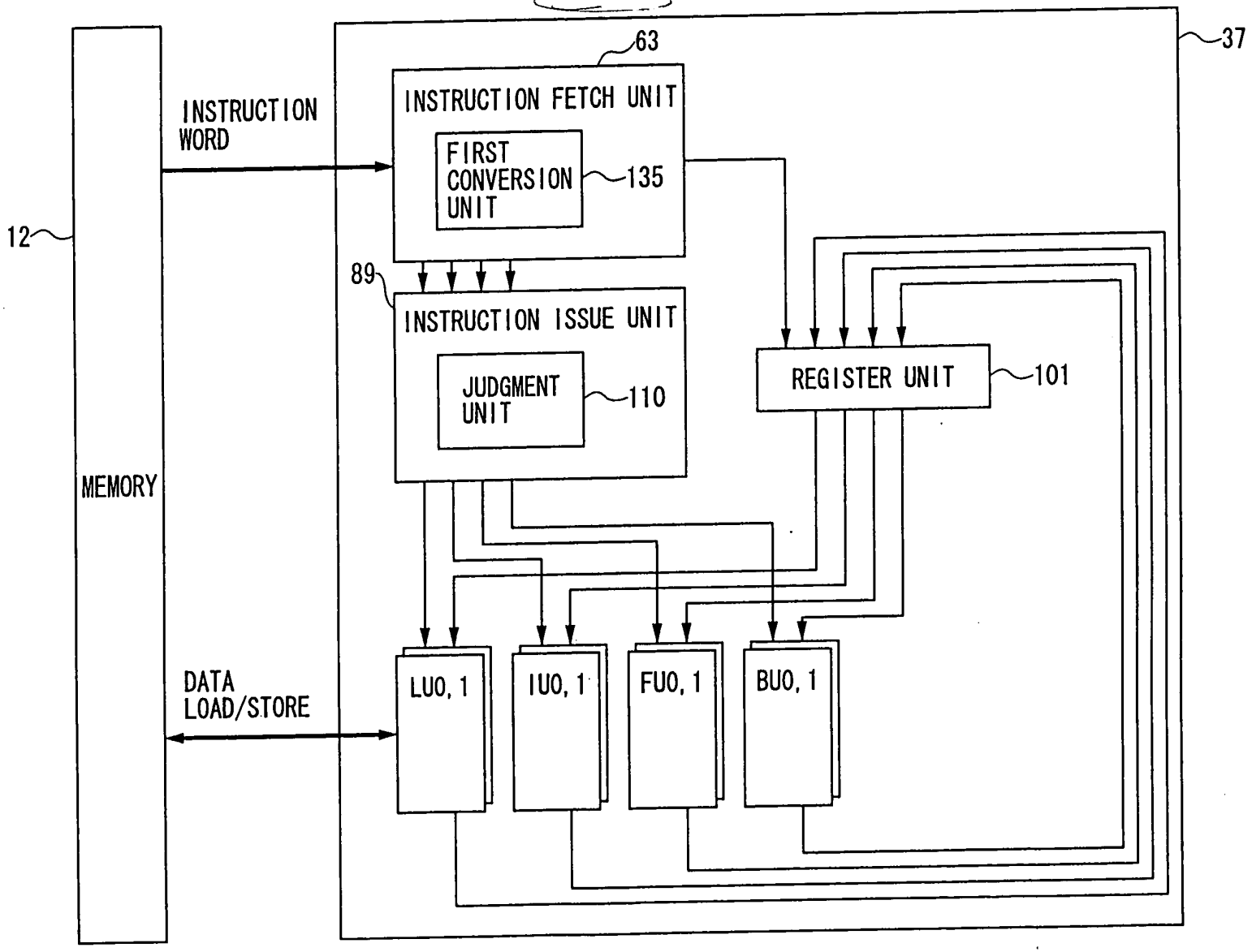
FIG.30



~~[FIG. 31]~~

Structure of a fourth example of the parallel processor in accordance with the fourth embodiment of the present invention

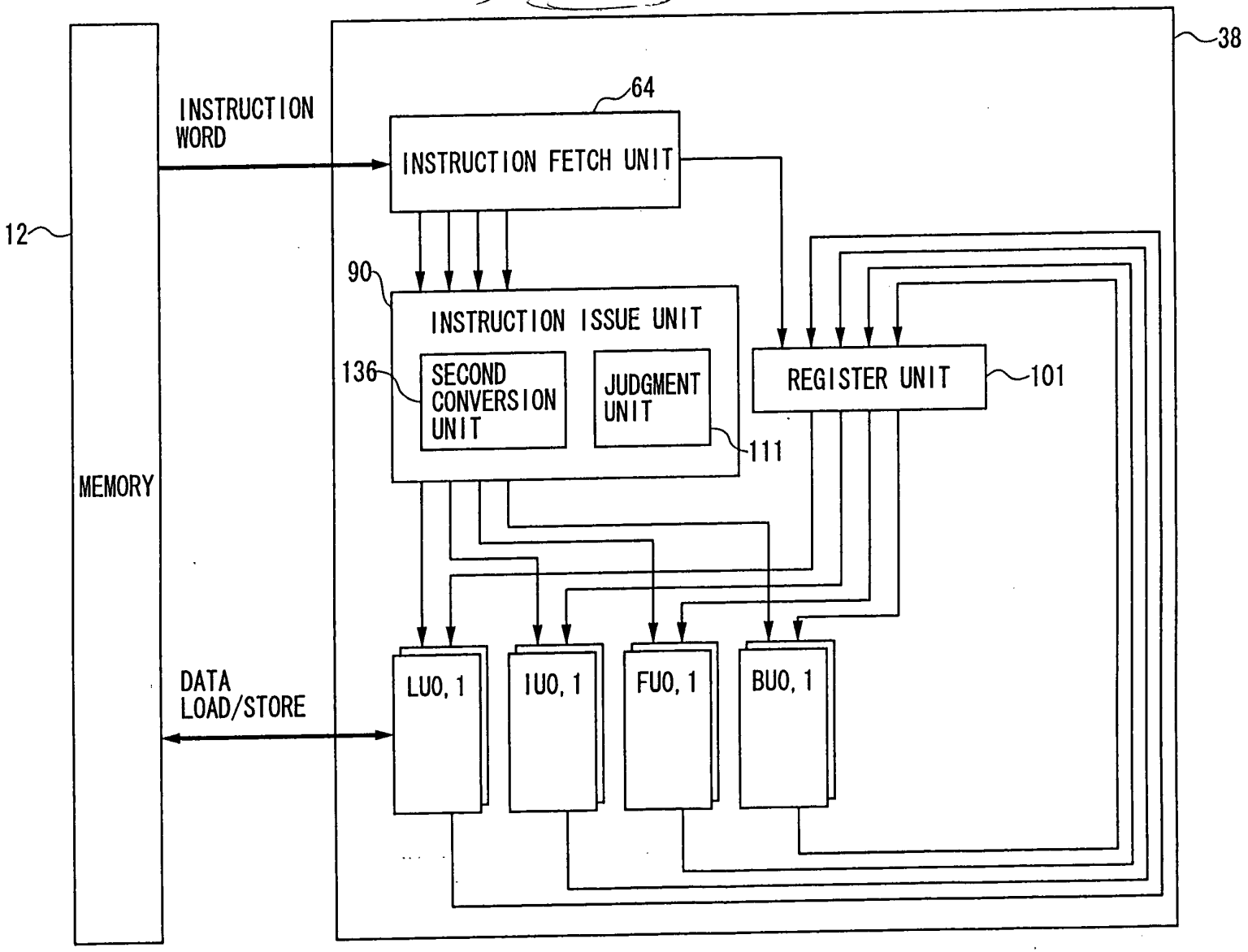
FIG.31



~~[FIG. 32]~~

Structure of a fifth example of the parallel processor in accordance with the fourth embodiment of the present invention

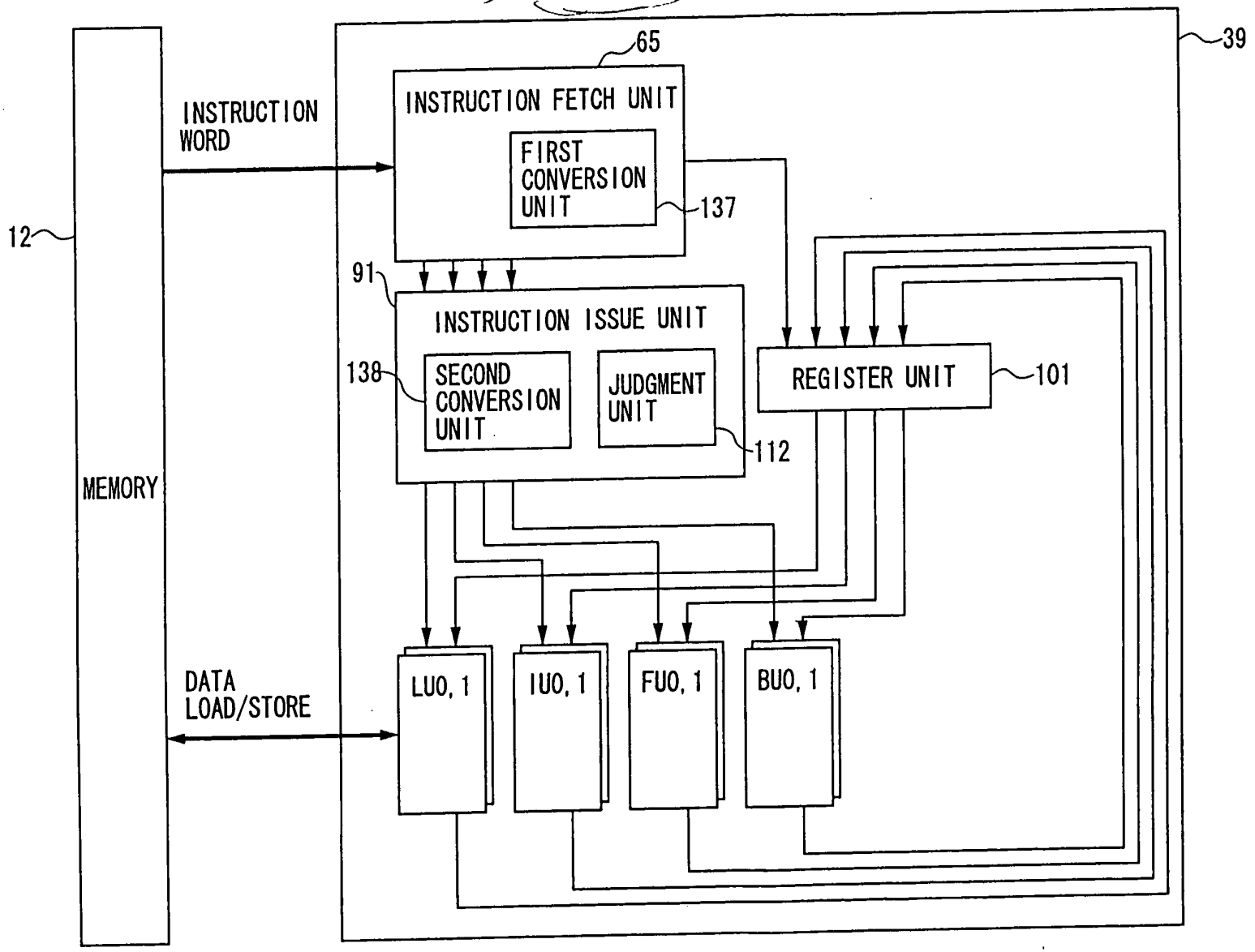
FIG.32



[~~FIG. 33~~]

Structure of a sixth example of the parallel processor in accordance with the fourth embodiment of the present invention

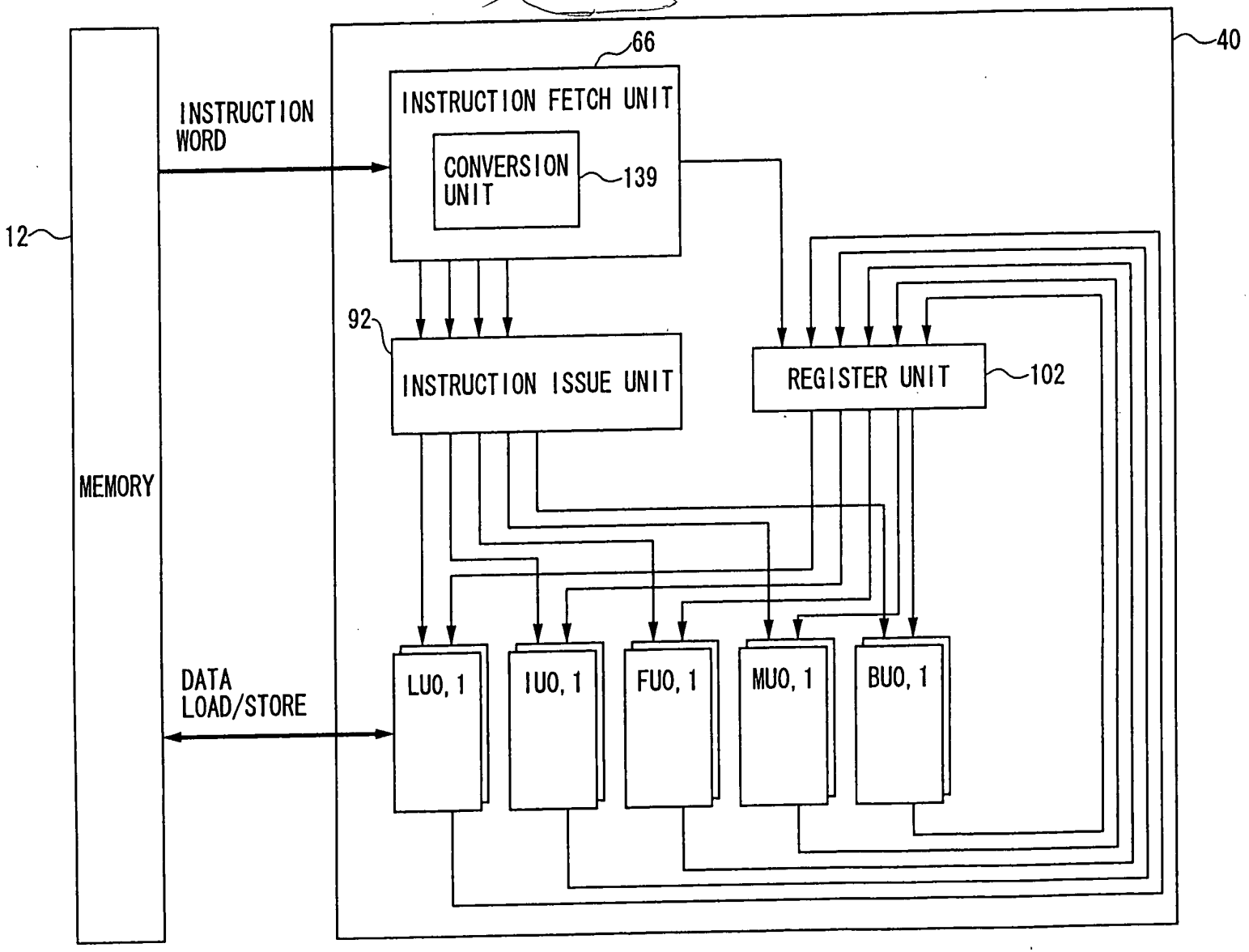
FIG.33



[~~FIG. 34~~]

Structure of a first example of a parallel processor in accordance with a fifth embodiment of the present invention

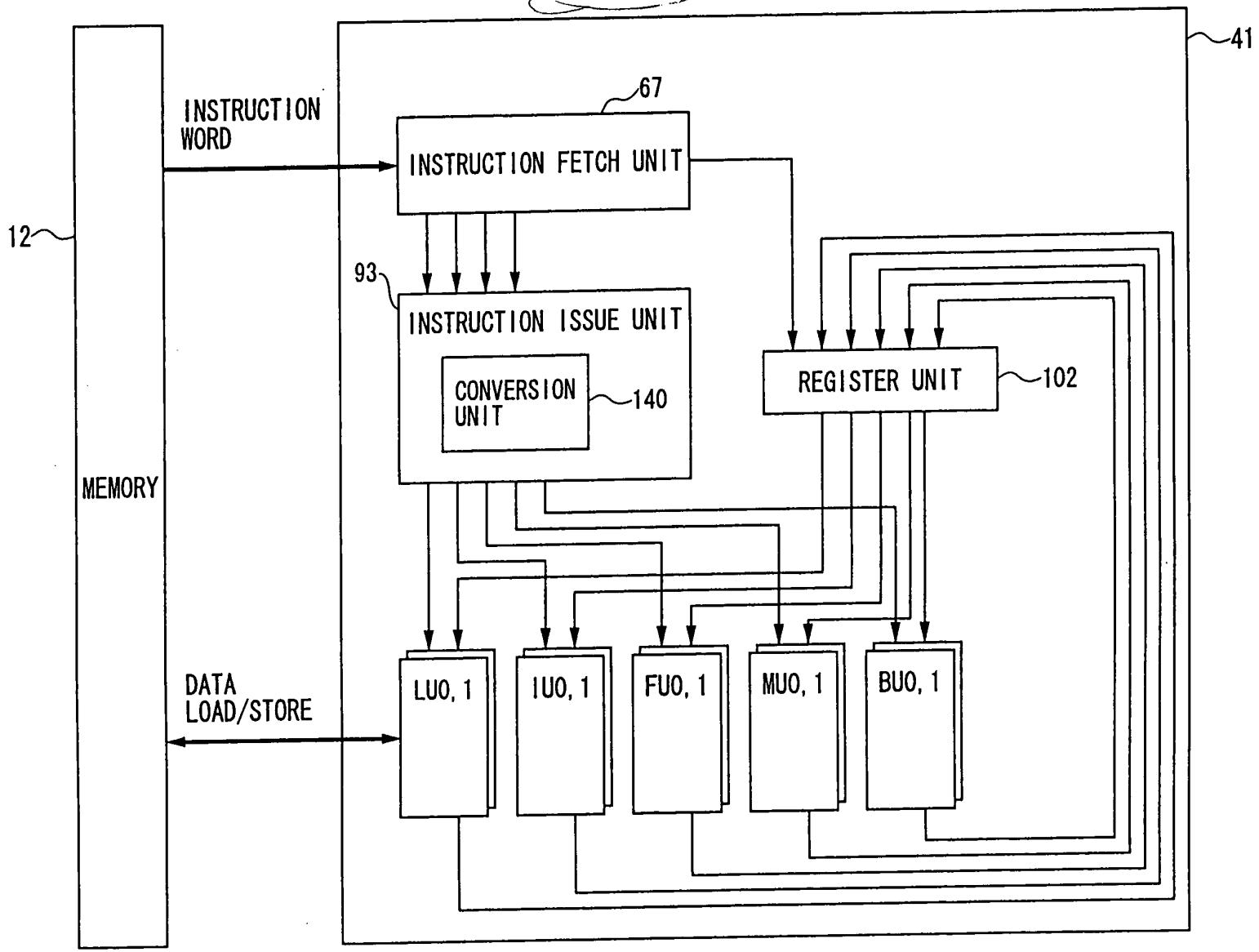
FIG.34



[~~FIG. 35~~]

Structure of a second example of the parallel processor in accordance with the fifth embodiment of the present invention

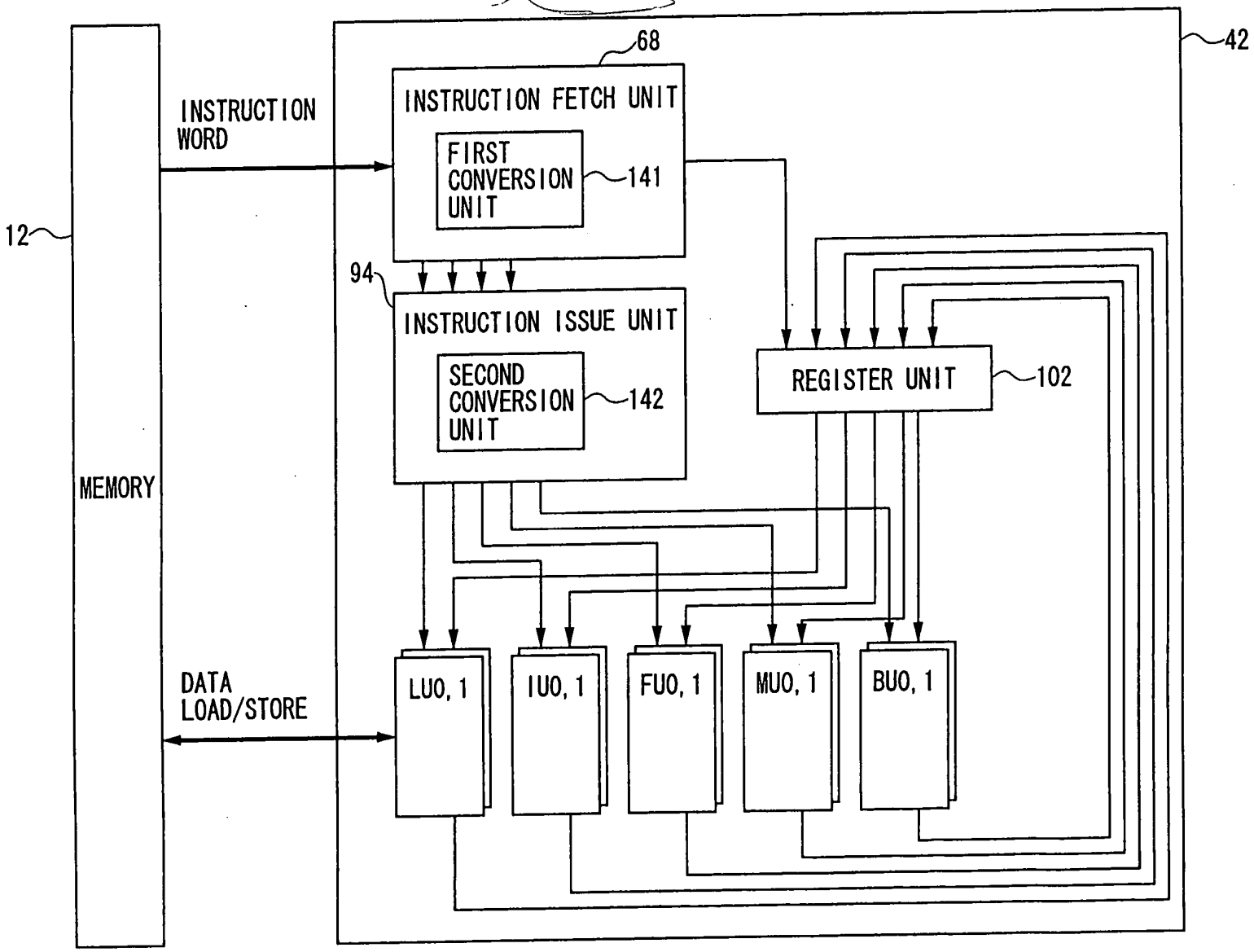
FIG.35



~~FIG. 36~~

Structure of a third example of the parallel processor in accordance with the fifth embodiment of the present invention

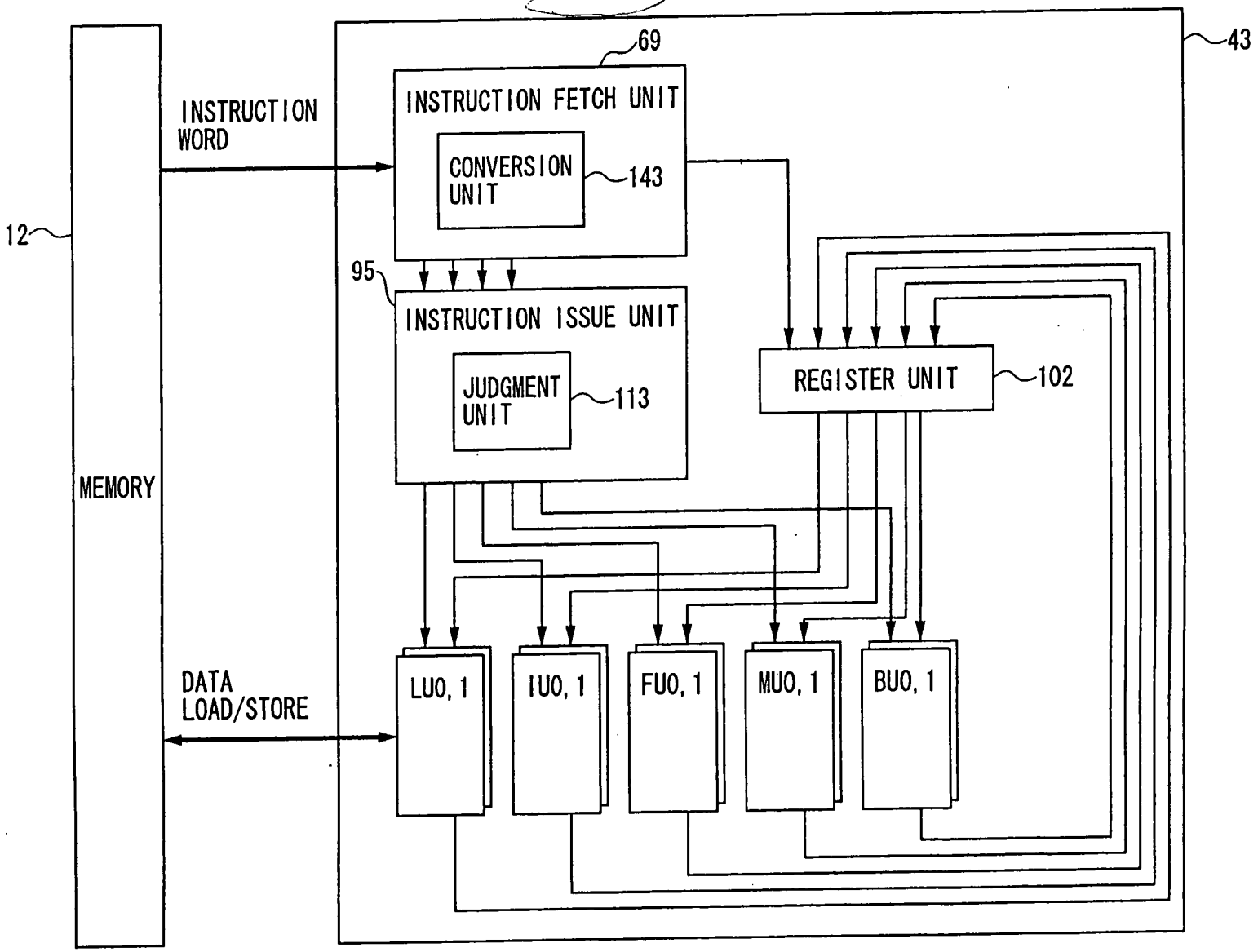
FIG.36



[~~FIG. 37~~]

Structure of a fourth example of the parallel processor in accordance with the fifth embodiment of the present invention

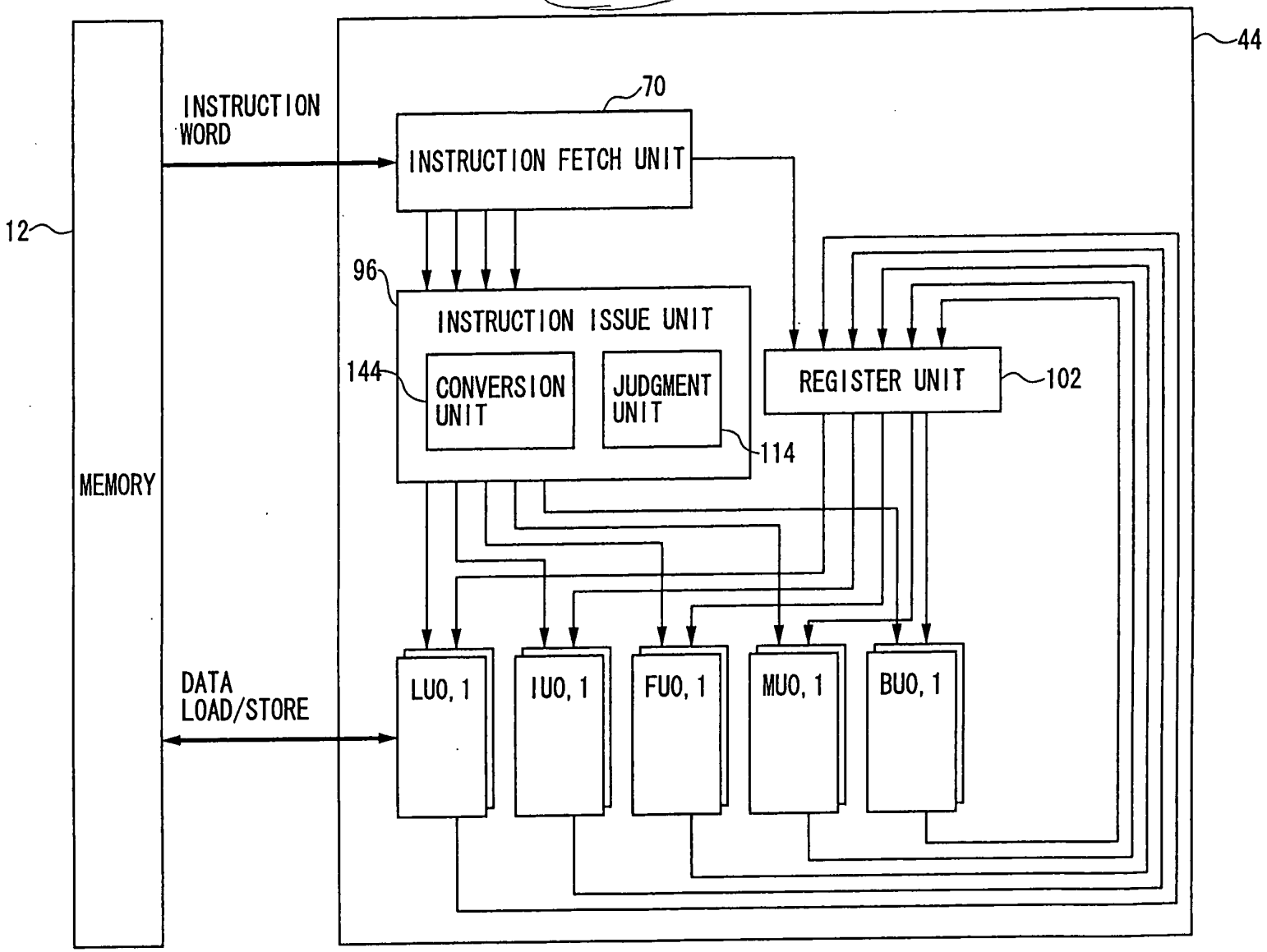
FIG.37



~~[FIG. 38]~~

Structure of a fifth example of the parallel processor in accordance with the fifth embodiment of the present invention

FIG.38



[FIG. 39]

Structure of a sixth example of the parallel processor in accordance with the fifth embodiment of the present invention

FIG.39